Michael Raab

„Technologie der Mikroelektronik der Schlüssel für die digitale Revolution“

Dresden, 19.März 2015

1MDRAM Speicherchip aus Dresden

Bild 10: Der Dresdner Megabit-Speicherchip U61000, 1988;
Lithografie-Niveau 1 µm, Chip 5,1 mm mal 12,85 mm, ca. 2,2 Mio Bauelemente

Chipfläche 65.5mm2

AMD – Jerry Sanders
„It is all about people“

First full functional 1MDRAM August 1988

Estimated number of produced parts in Dresden: 30kdice between Sept 1988 and 1990
Development without economical effect but

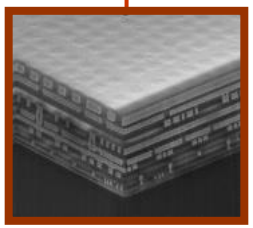
Technology 1MDRAM-1µm (1988) vs 32nm (2010)

Scaling by factor of ~30 in 22years, 10Tech Nodes in between

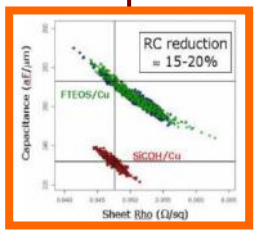
Si Substrate (125mm wafer)	SOI Substrate (300mm wafer)
16 mask layer (6 Implants)	55 mask layer (20 Implants)
1 Layer of Metal (Al/Si)	11 Layers of Metal (Cu)
Poly Silicon Gate	HK Metal Gate
MoSi Bitleitung	5th Gen Strained Silicon
Gate Length: 1000nm	Gate Length: 35nm
DRAM Cell Size = 32.4µm^2	SRAM Cell Size = 0.258µm^2

High Advanced Technologies in Dresden

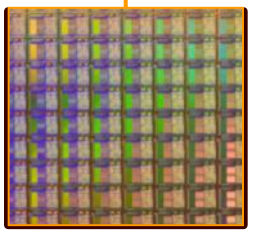
2000	2002	2003	2004	2006	2008	2010
180nm	130nm	130nm	90nm	65nm	45nm	32/28nm



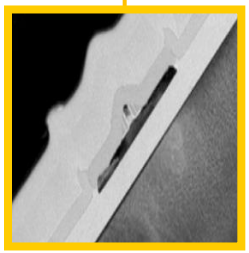
Cu Interconnect



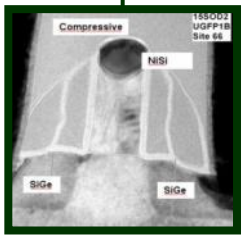
Low-K dielectric



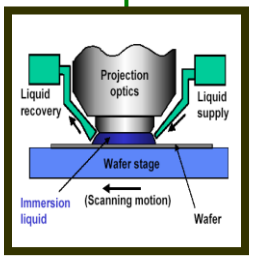
SOI



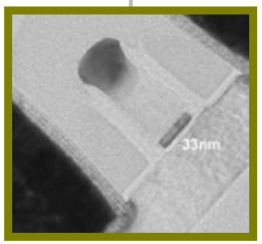
Strained-Si



Multi-Strain Transistor

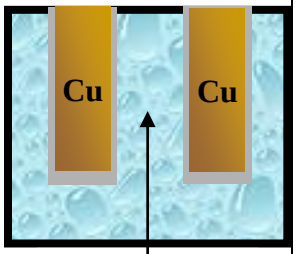


Immersion Lithography



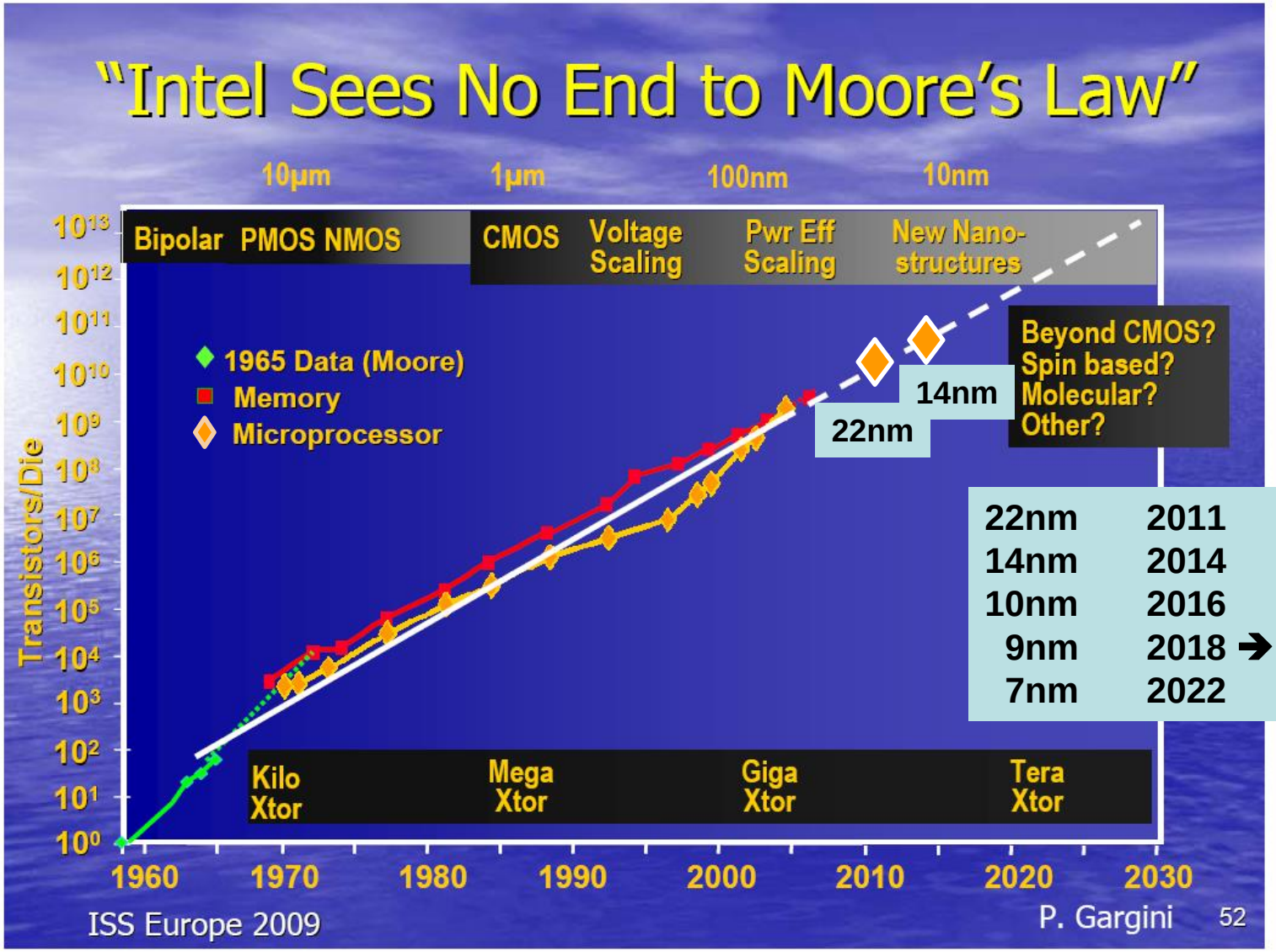
HKMG

- 8 technologies successfully developed through Joint Development Alliance and AMD/GLOBALFOUNDRIES collaboration
- All technologies run in high volume manufacturing
- 32nm and 28nm volume manufacturing at GLOBALFOUNDRIES
- **Further scaling in GLOBALFOUNDRIES-Dresden only with EU and Germany funding, support and focus**



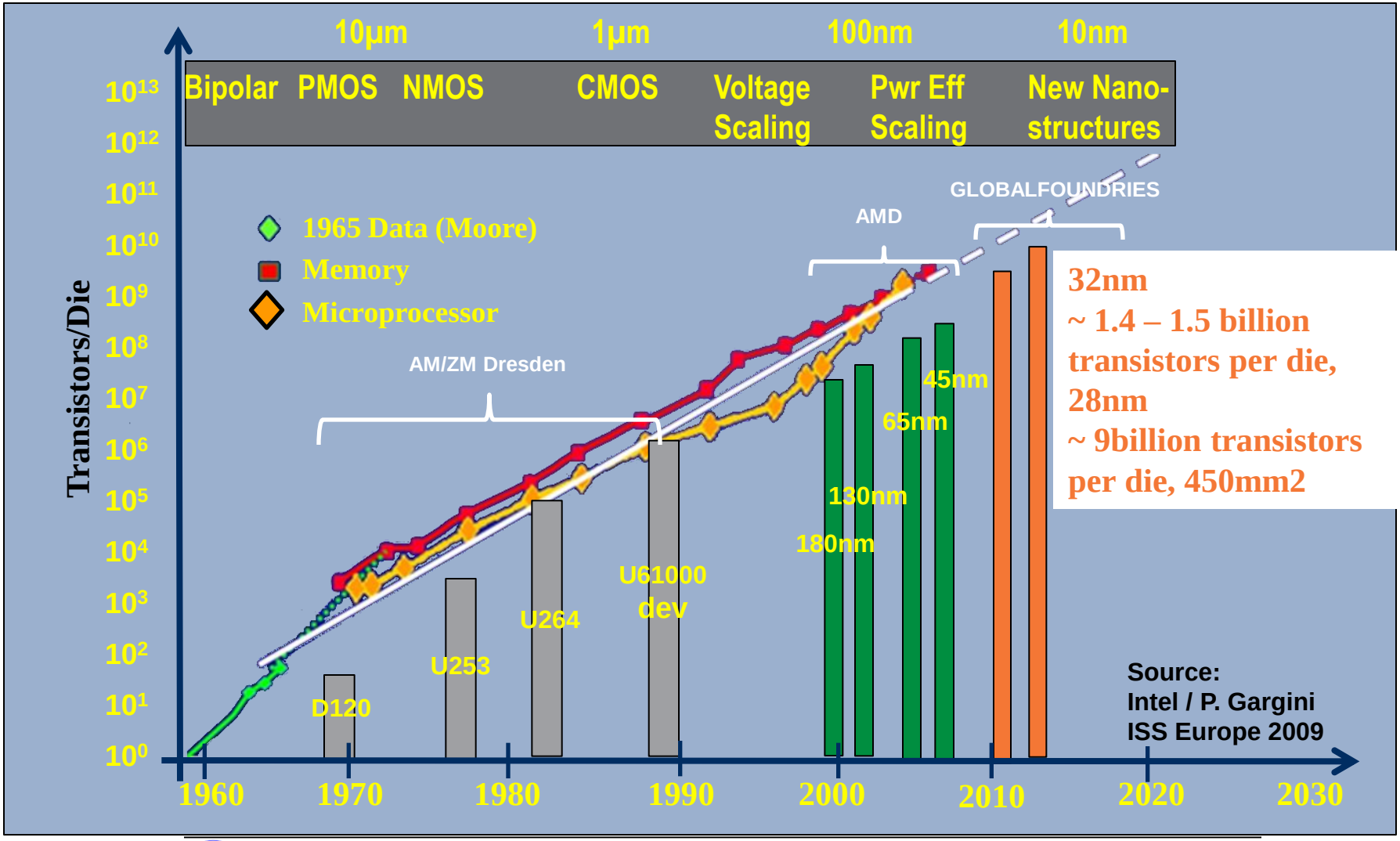
ULK

ITRS Roadmap

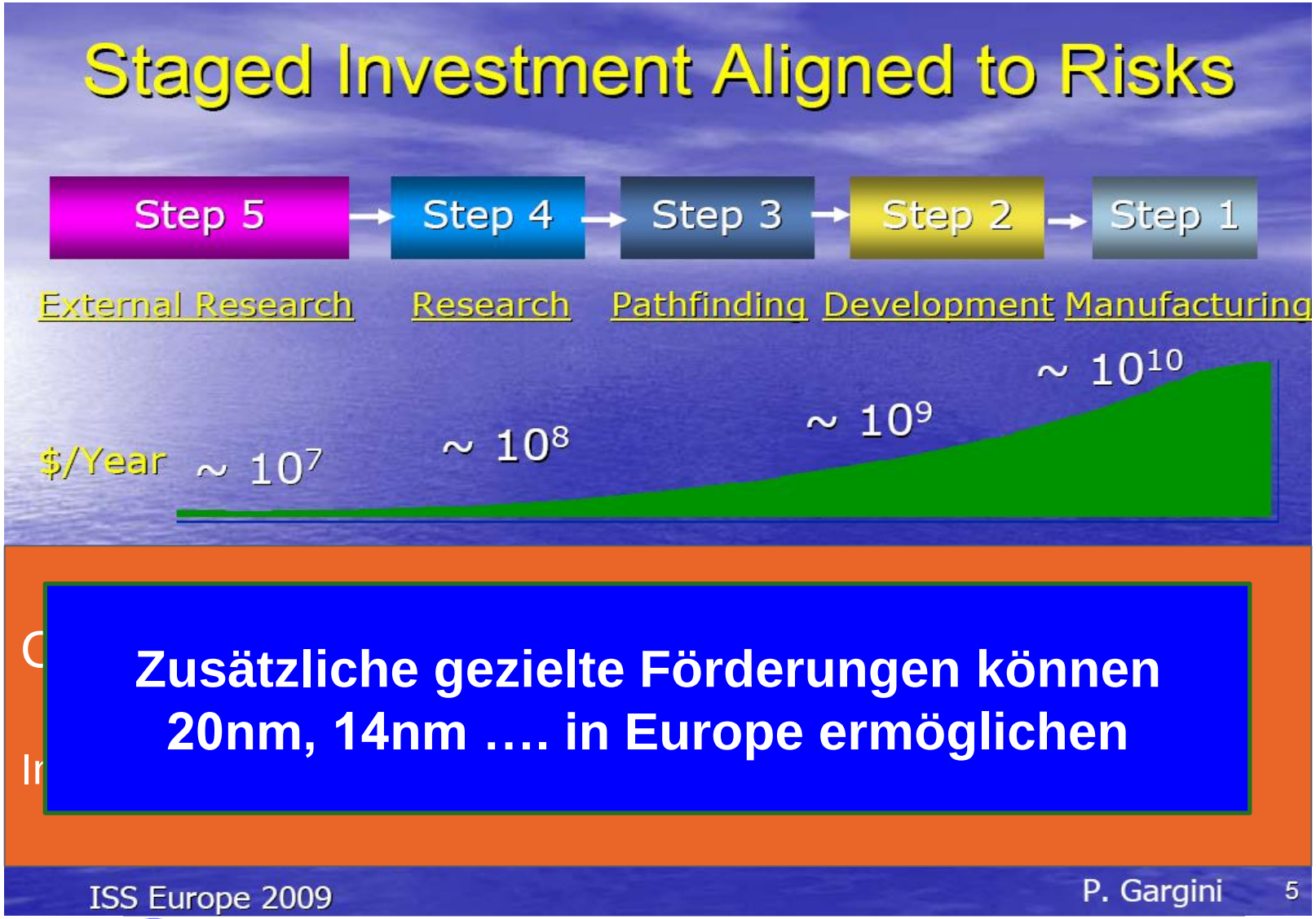


22nm	2011
14nm	2014
10nm	2016
9nm	2018 ➔ 2019
7nm	2022

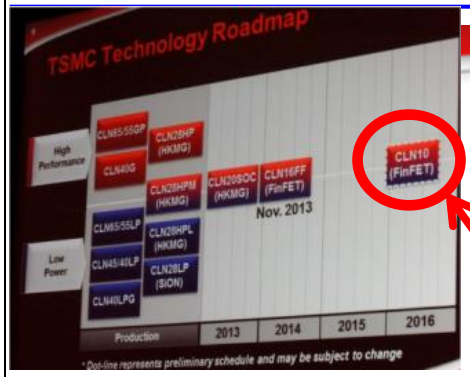
From Bipolar to CMOS at highest performance



Mikroelektronik Aufwand



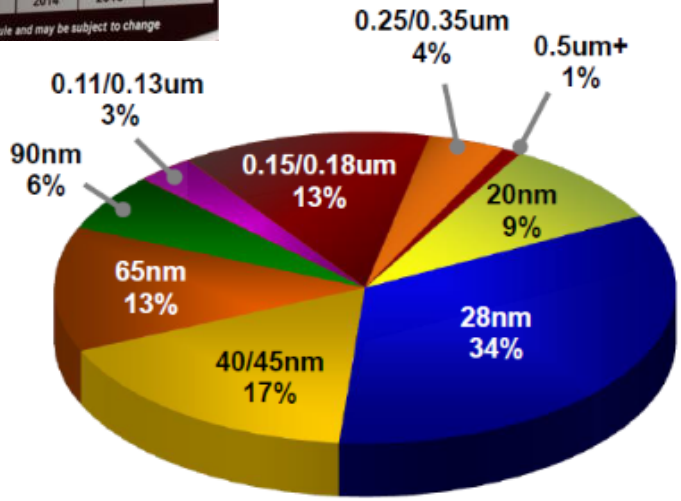
TSMC Revenue to change from 28nm → 20nm

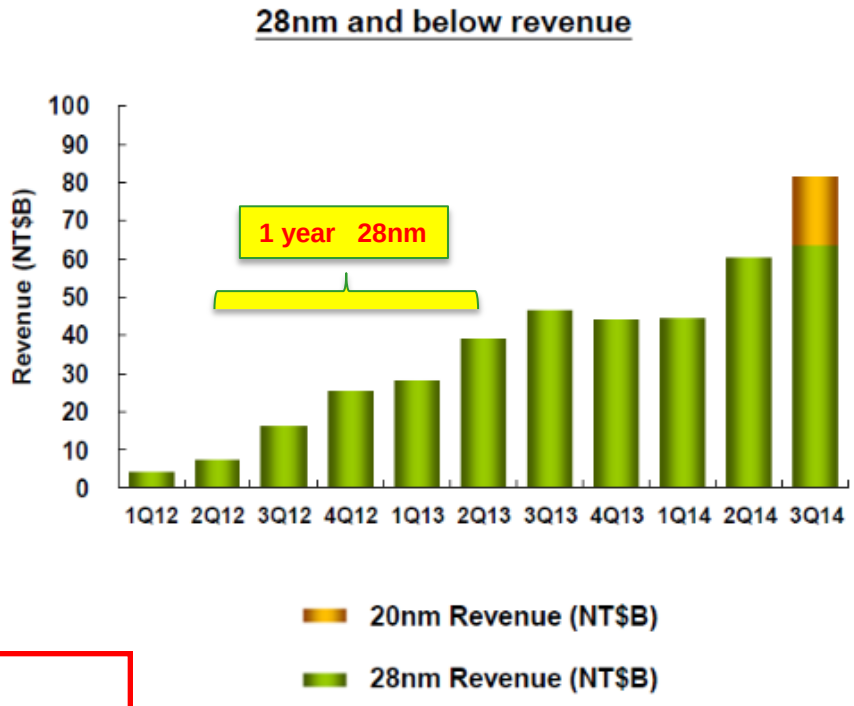


10nm in 1H2016

3Q14 Revenue by Technology

TSMC Property

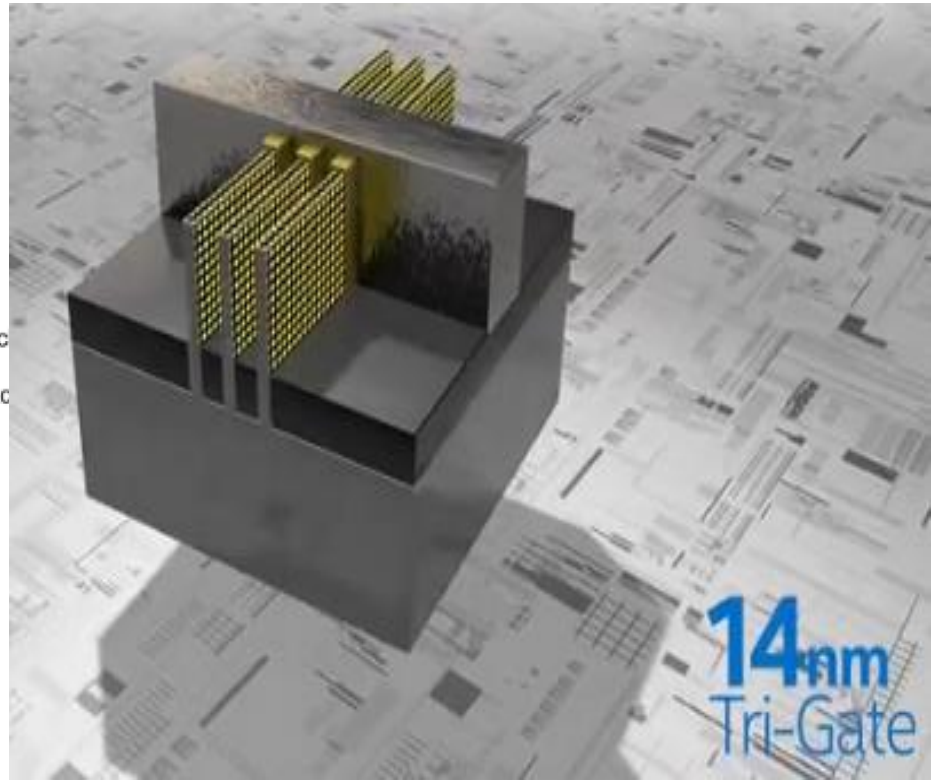




Don't stop development followed by production

INTELs 14nm Technology with 2nd-Generation FINFET

Gate Pitc
x
Metal Pitc
(nm²)



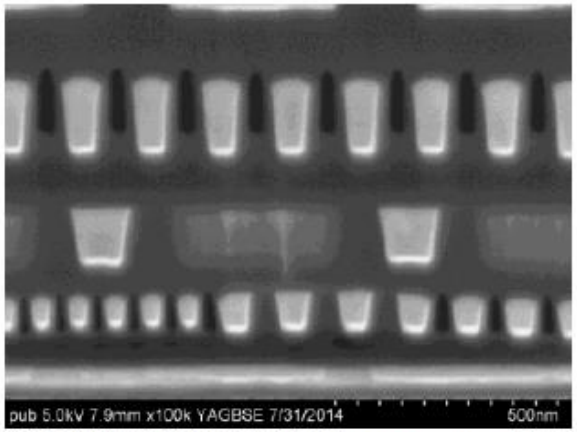


Figure 11: Air-Gapped Interconnects

Layer	Pitch (nm)	Scale Factor to [1]
Fin	42	0.70
Contacted Gate Pitch	70	0.78
Metal 0	56	N/A
Metal 1	70	0.78
Metal 2	52	0.65

Table 1: Layer Pitches

Self-Aligned Double Patterning, 0.0588µm2 SRAM cell size

- 4th generation high-k metal gate, and 6th-generation strained silicon
- Idsat improvement of 15% for NMOS and 41% for PMOS over 22nm
- 42nm fin and 70nm contacted gate pitch Idsat are 1.04mA/µm at Vdd 0.7V
- Slopes are maintained at ~65mV/decade; DIBL is ~60mV/V and ~75 mV/V for NMOS and PMOS, respectively

IEDM2014

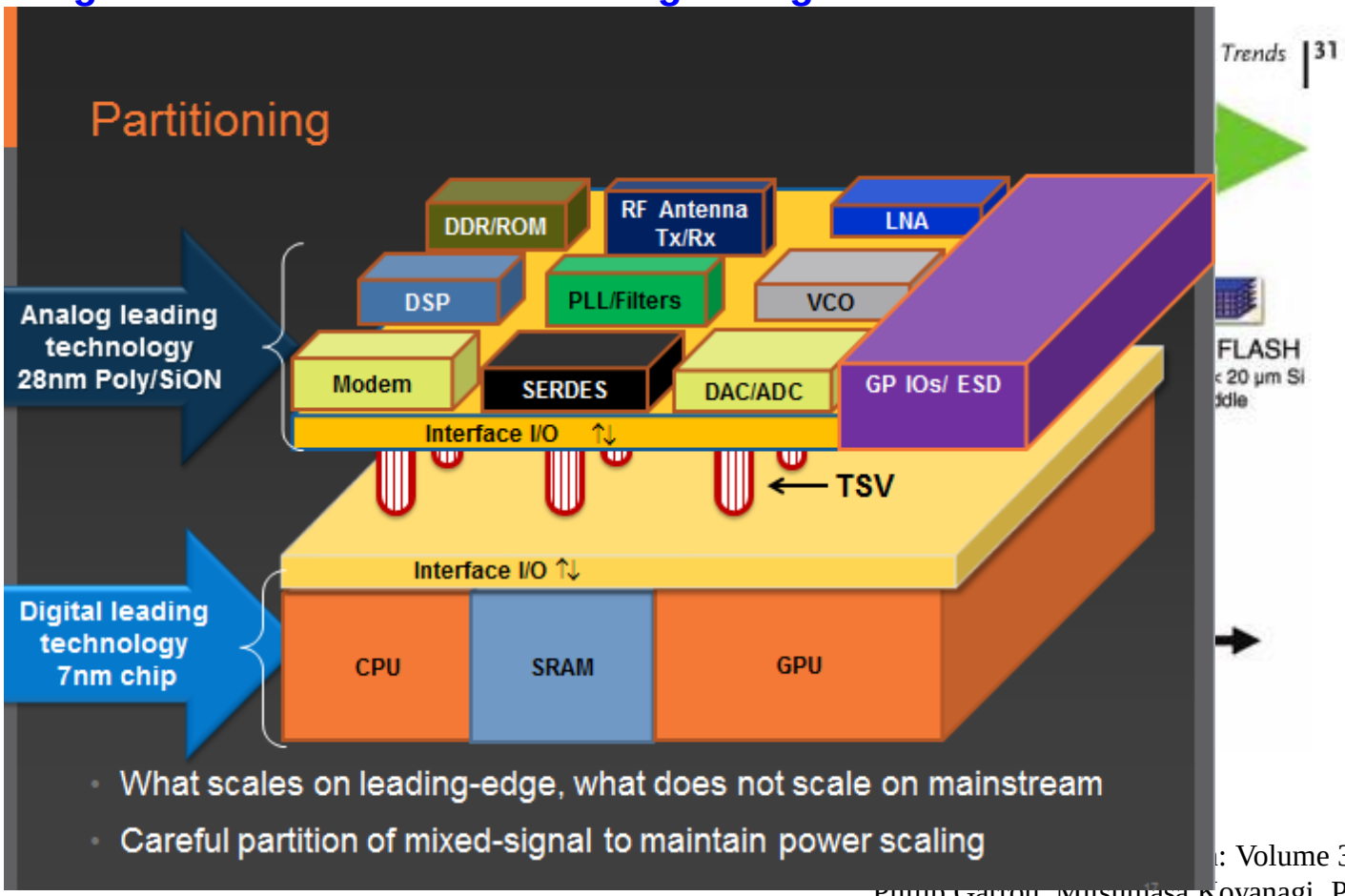
Halbleitermarkt: das Herz für komplexe Systeme

Sector Market Size in US$

Interposer or TSV

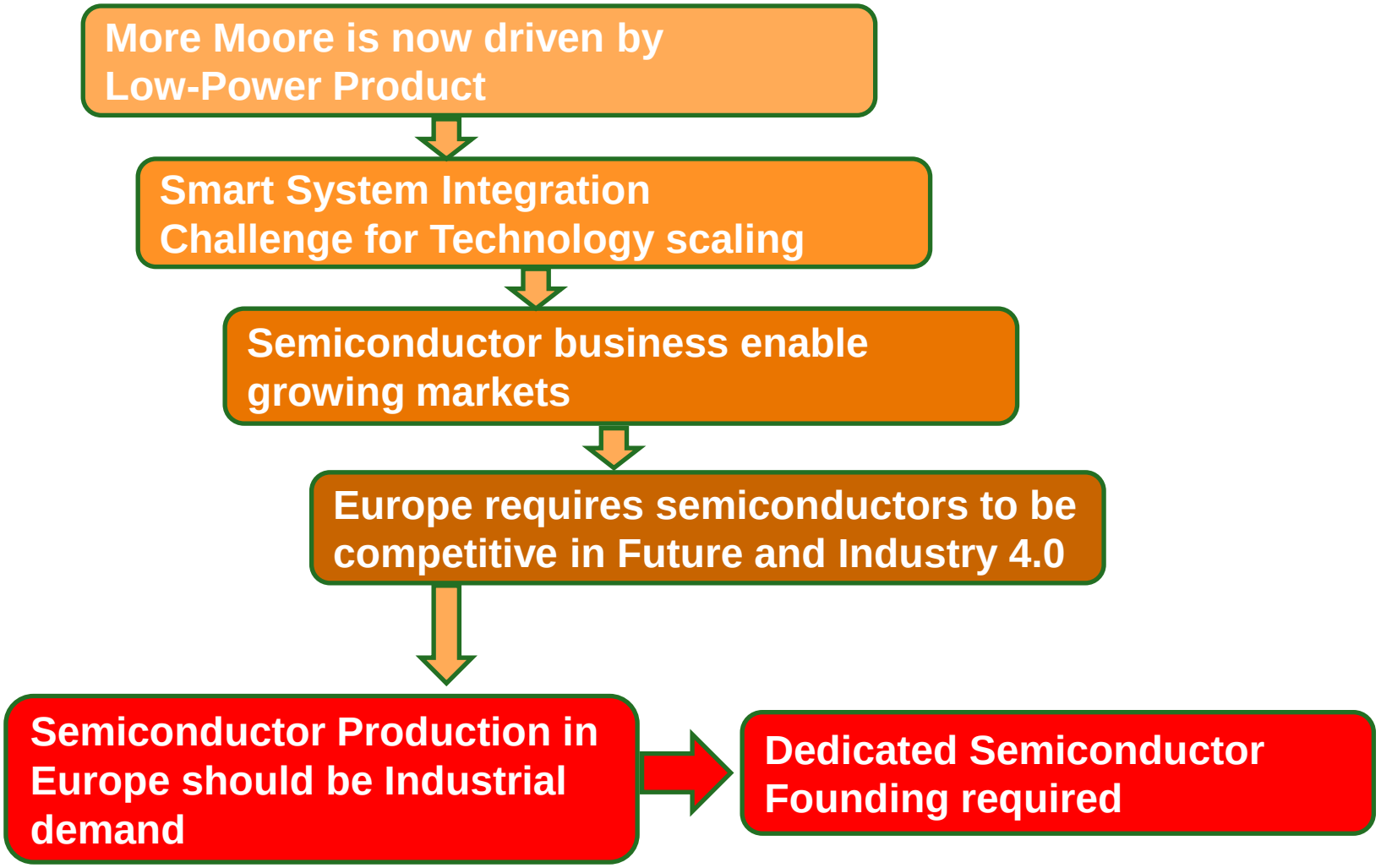
Internationale Roadmap mit klaren System-Vorstellungen und 3D-Integration

SoC auch mit Interposer oder TSV
nur gemeinsam mit Basistechnologie möglich



: Volume 3 - 3D Process Technology
Philip Garrou, Mitsumasa Koyanagi, Peter Ramm

Technology Summary enabling Industrial4.0



EU - Zielstellung

EU-Ziel: 20% Mikroelektronik Fertigung in Europa bis 2020

Notwendiger Schritt zur Umsetzung

Investition einer neuen 300mm Linie für 14…7nm Technologie in Europa