Jörg Ludewig

„Speicherchip-Packaging – die Technologielokomotive für das Back-end"

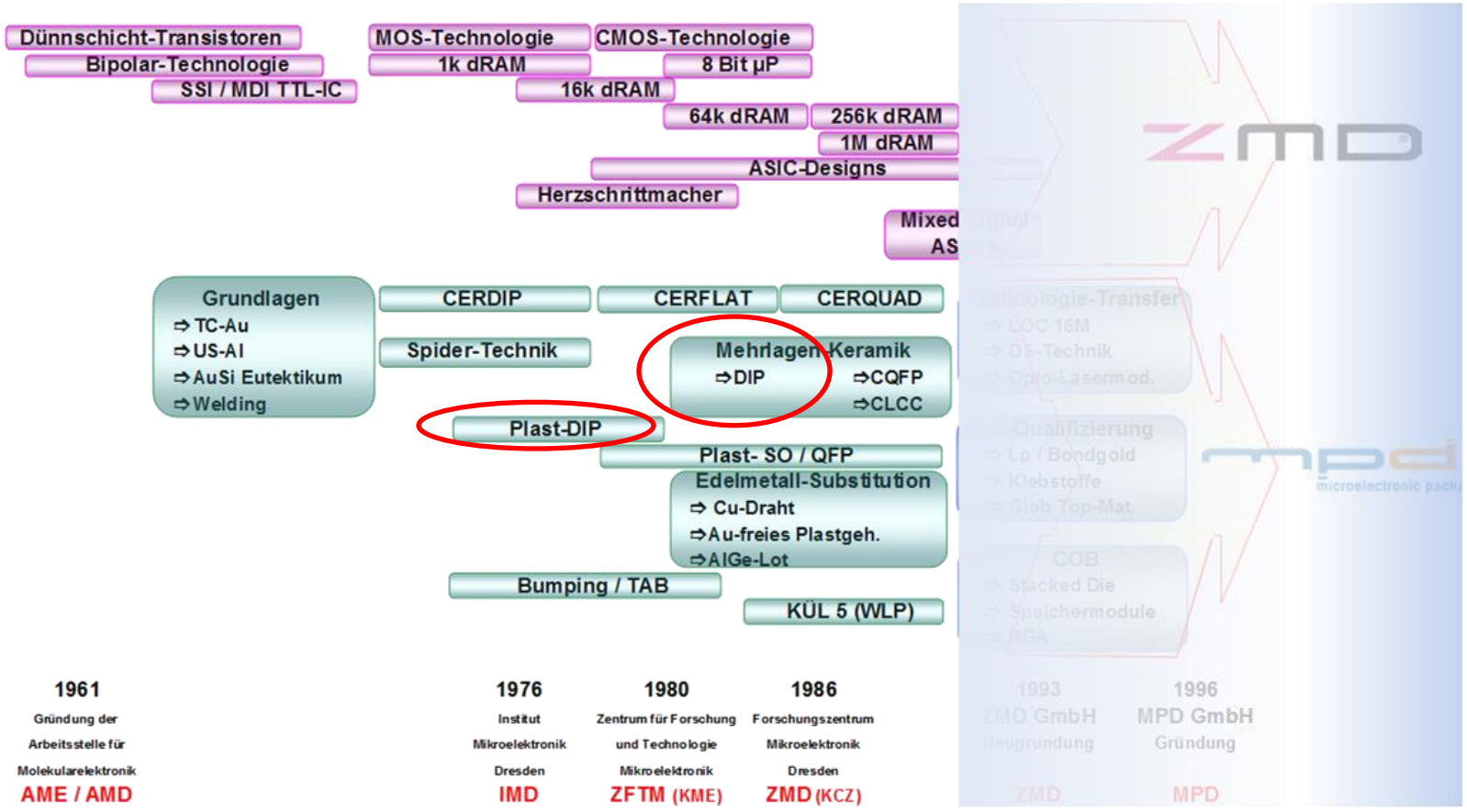
Dresden, 19.März 2015

1 M Speicher

- Anforderungen an Gehäuse 1 M Speicher
  - Bauform DIP 18
  - Reihenabstand 7,5 mm
  - Plast
  - Keramik
  - Standard-Montagetechnologie mit ggf. Chip-Schutz

1 M Speicher

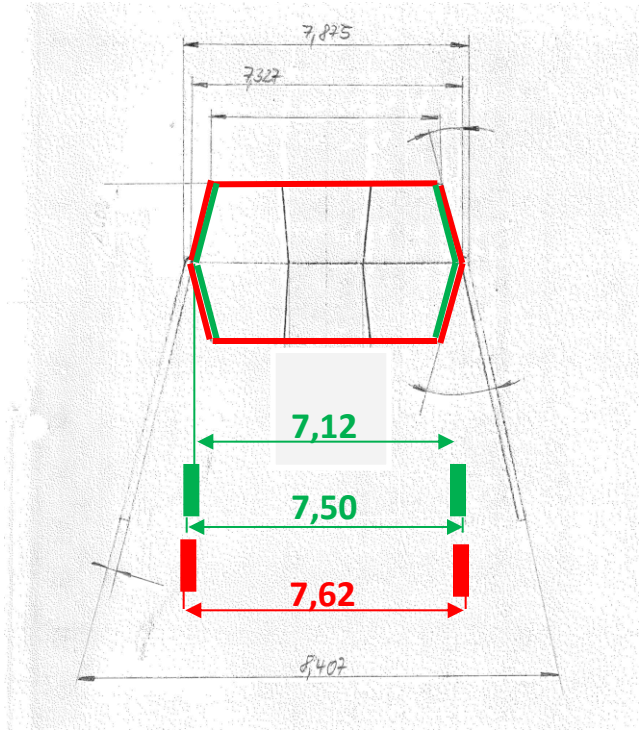
- Entwicklung in Dresden

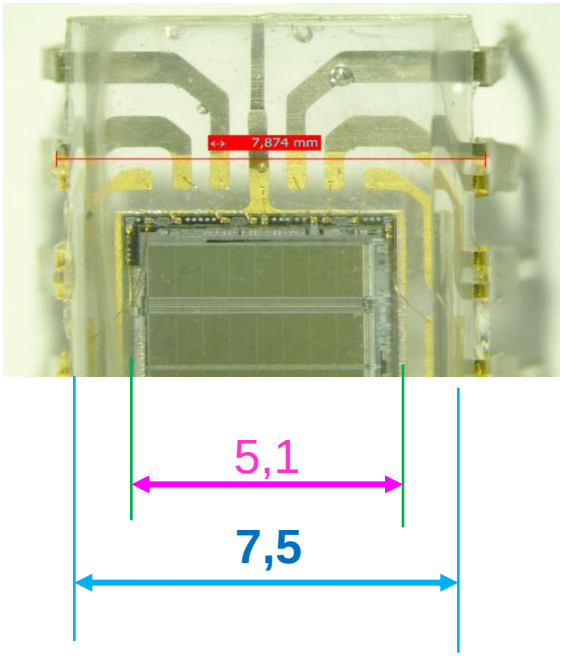


1 M Speicher

- Fremdmuster

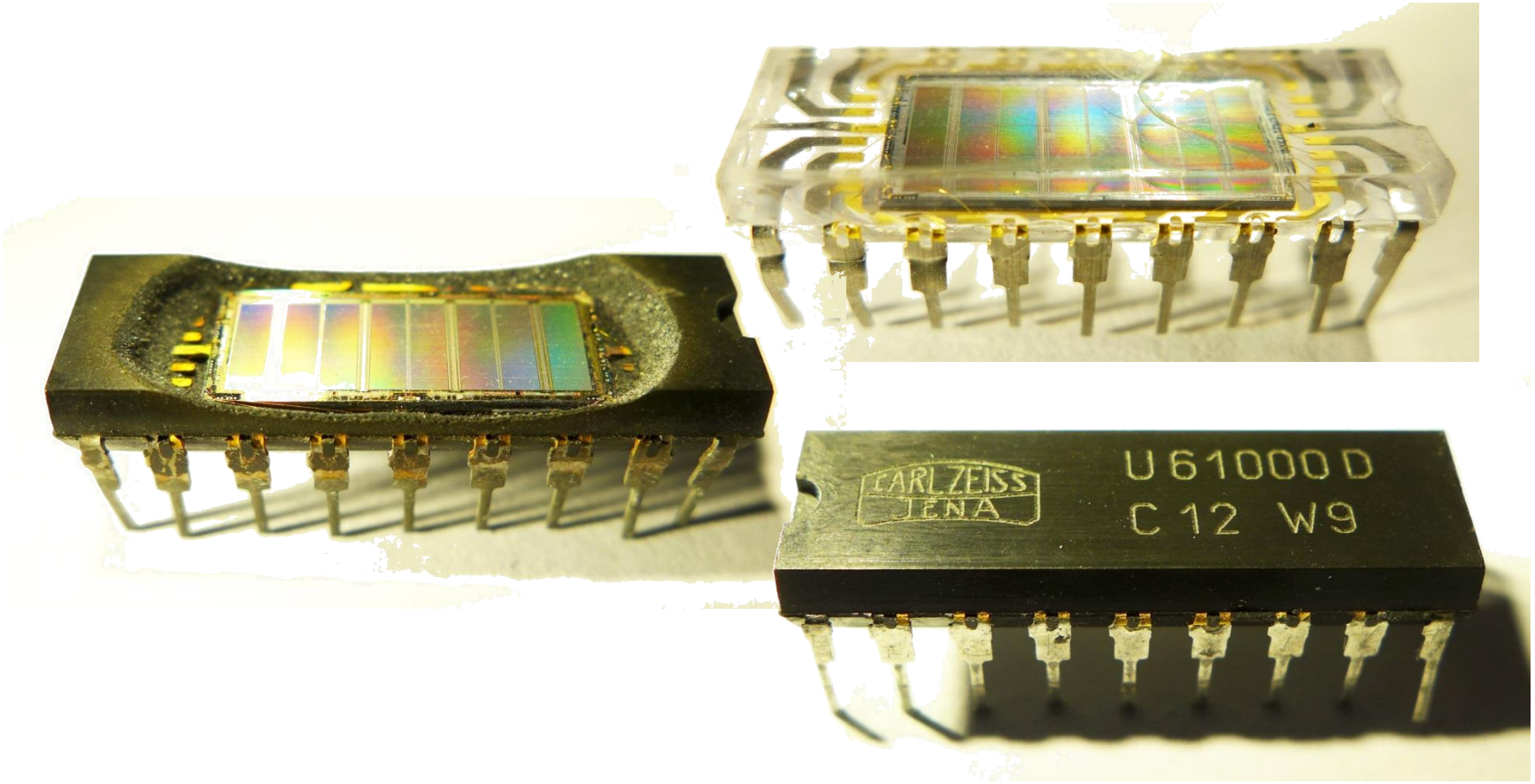
ZMD





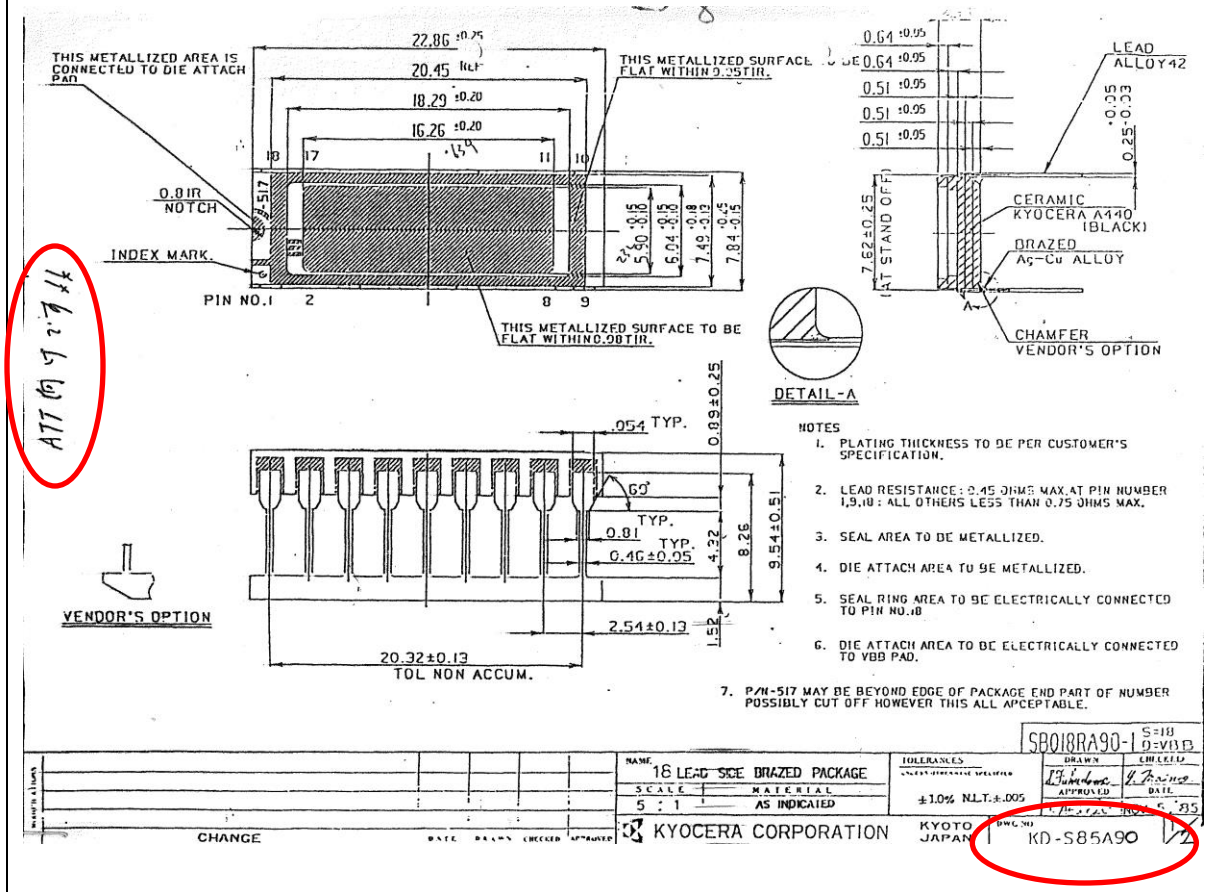
1 M Speicher

- Eigene Lösung DIL-Plast



1 M Speicher

- DIP MK 18



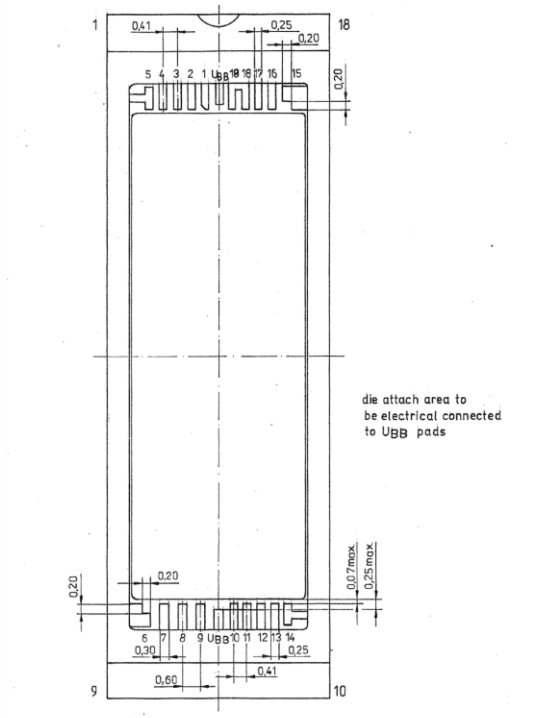
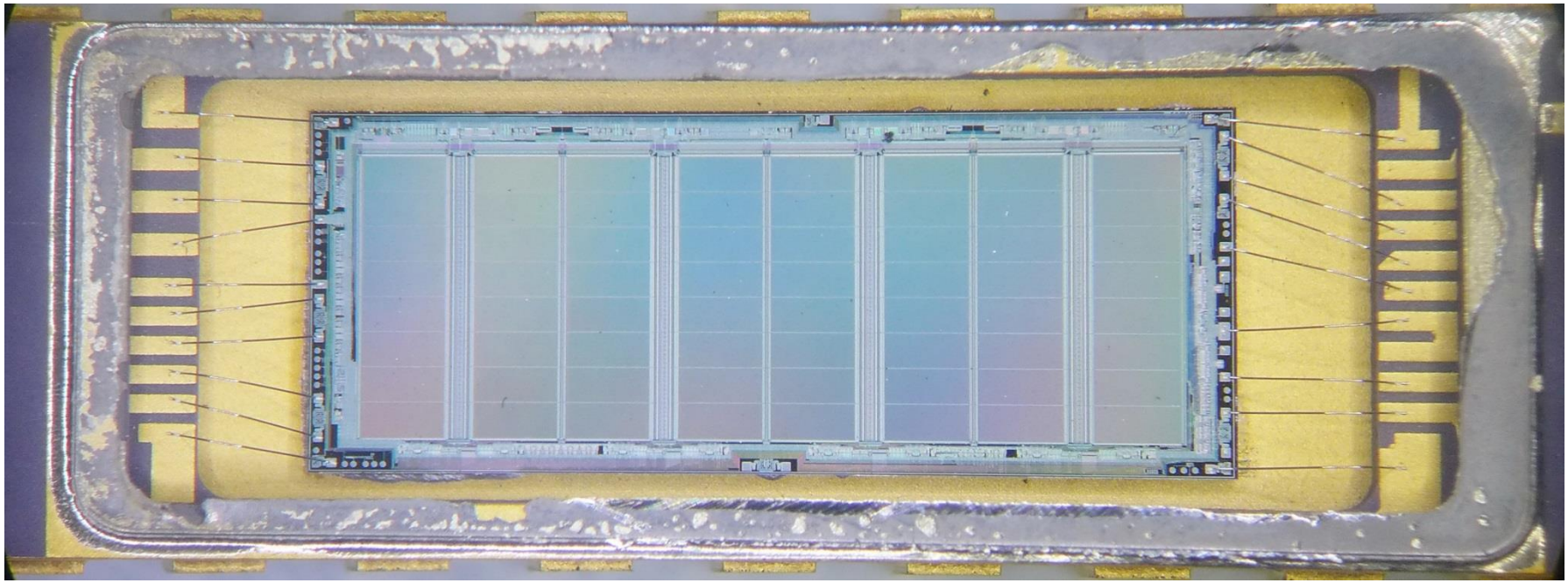


figure 1: modification for bondingfinger layout for KD S 85 A 90

1 M Speicher

- Eigene Lösung DIK MK 18



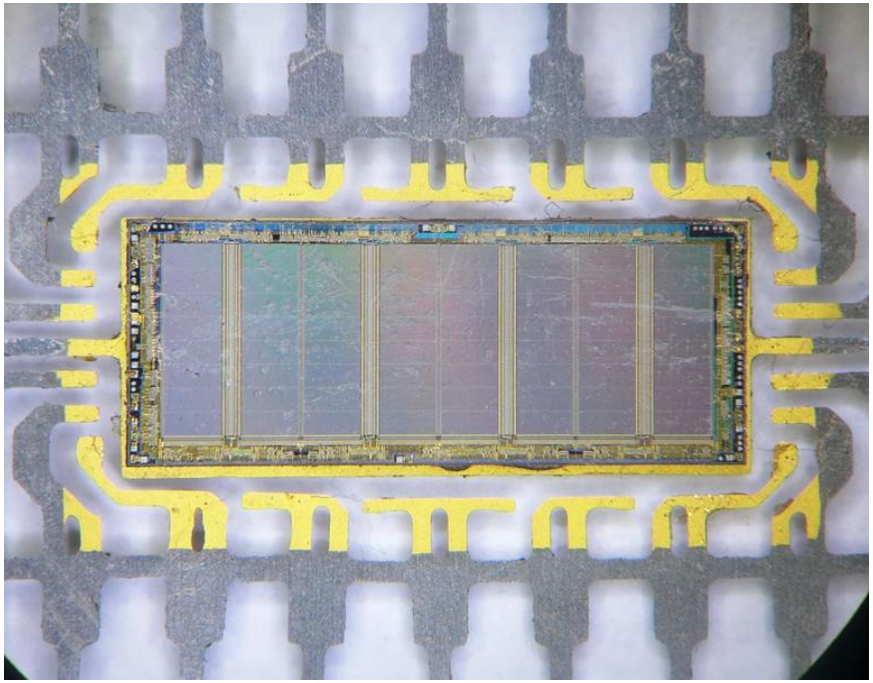
Packageentwicklung Speicher

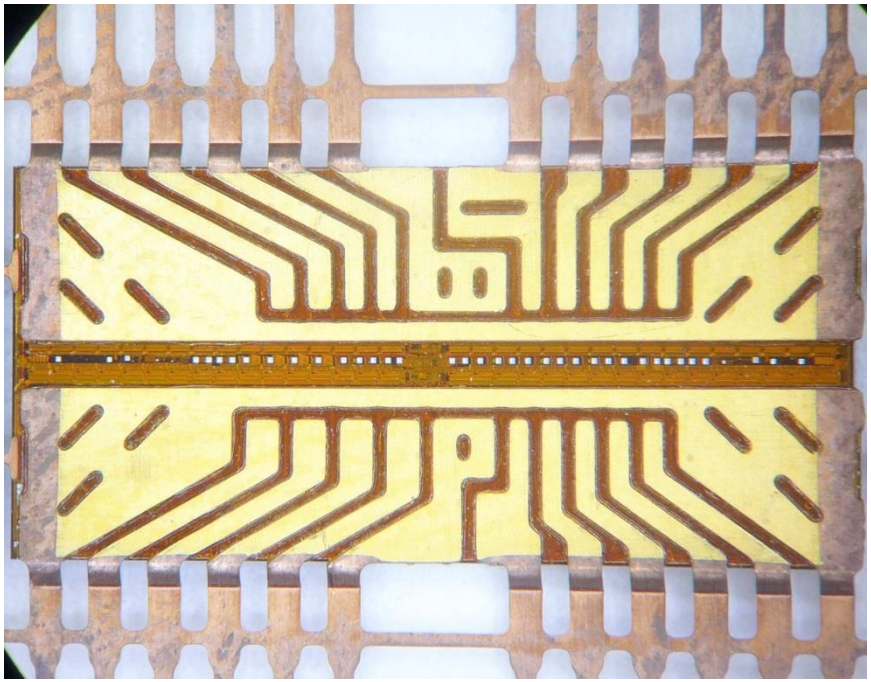
- Packageentwicklung
  - Bauform / Montagetechnologie / Padlayout

Bauform	DIP / SO	SO / TSOP	TSOP / FBGA	FBGA	FBGA
					
Montagetechnologie	TS-Standard	LOC BOC	LOC BOC	COB über RDL stacked	TSV stacked
Padlayout					
Chipdicke	350 µm	250 µm	200 µm		100 µm
Speicherkapazität	256 k/ 1M	16 M	1 G	> 1 G	> 4 G

Packageentwicklung Speicher

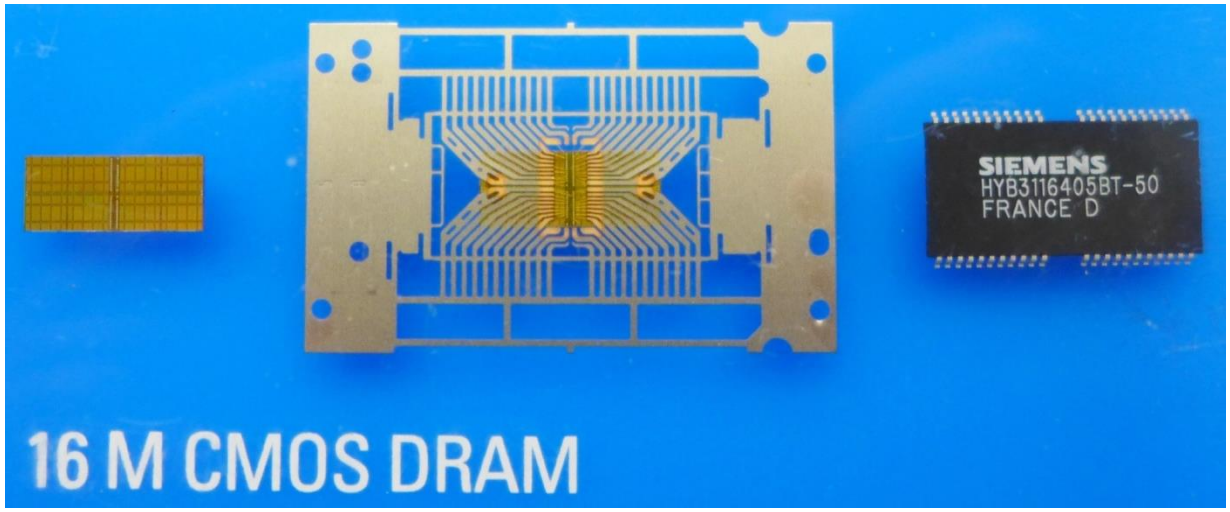
- Packageentwicklung DIP auf LOC

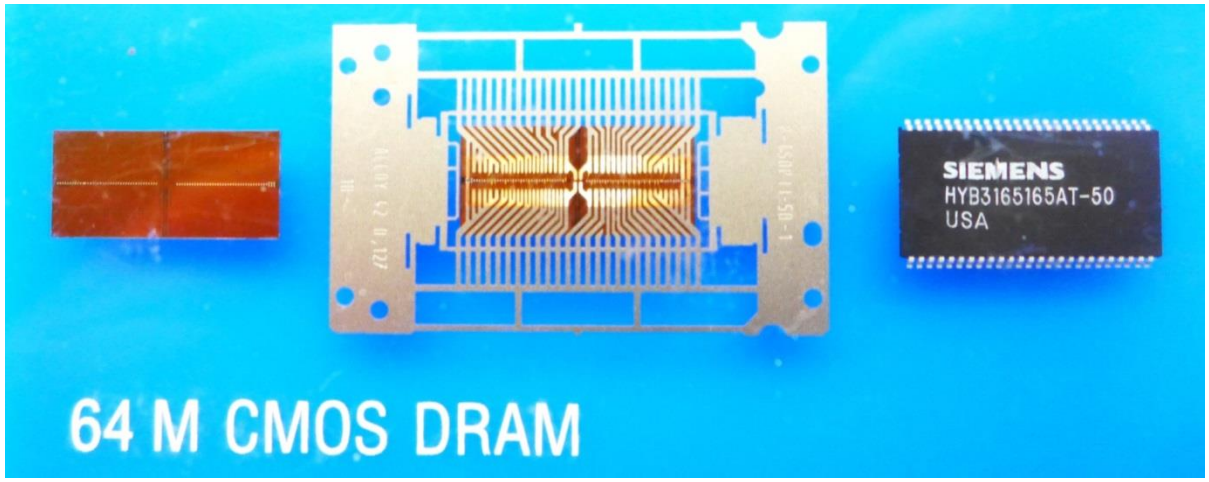




Packageentwicklung Speicher

- Packageentwicklung LOC





Quelle Siemens

Packageentwicklung Speicher

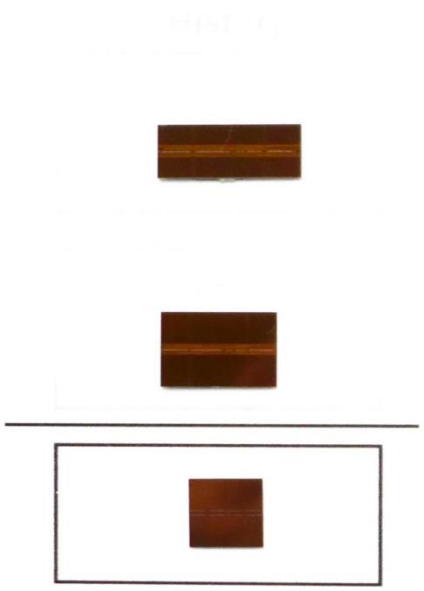
- Packageentwicklung BOC - FBGA

Qimonda

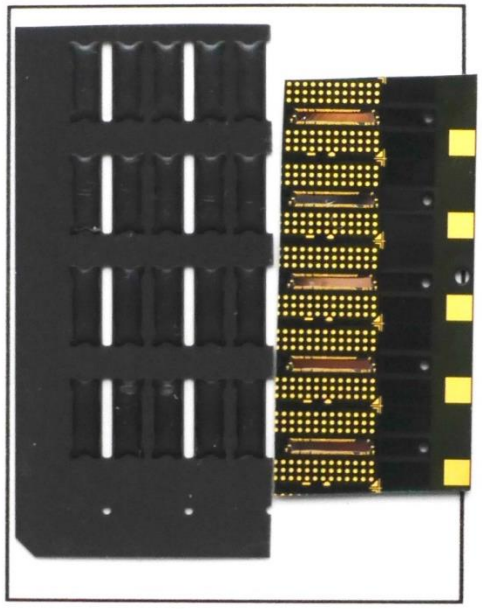
Last QD Backend Product

PG-TFBGA-78-151
PG-TFBGA-96-151

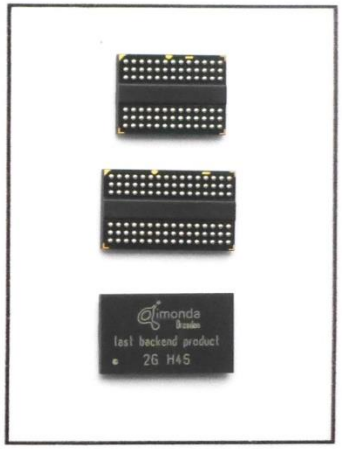
2G DDR3-SDRAM
H46
Substrate Step4



46 nm bWLTechnology
52,98 mm² Chip Area
(7,55 x 7,01) mm³



1L-BOC Substrate
Wedge Pad Pitch = 150 µm
Min Trace Width = 20 µm

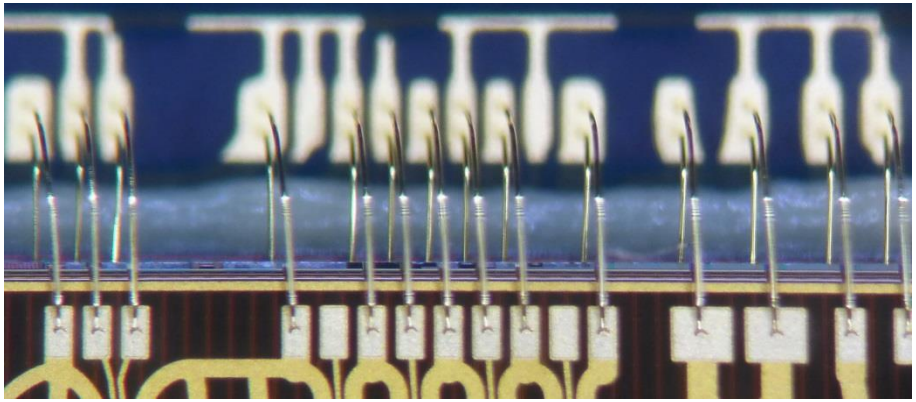


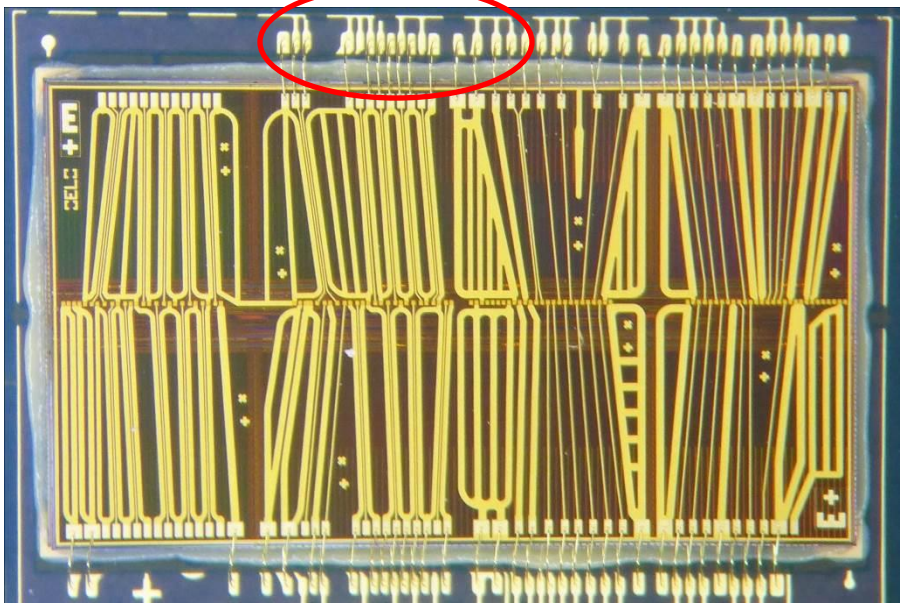
(8 x 13,5 x 1.2) mm³
(8 x 11 x 1.2) mm³
Ball Diameter 450 µm
Pitch (0.8 x 0.8) mm²

Quelle Qimonda

Packageentwicklung Speicher

- Packageentwicklung COB
  - Chip mit Umverdrahtung (RDL)
  - 2-fach Stapel





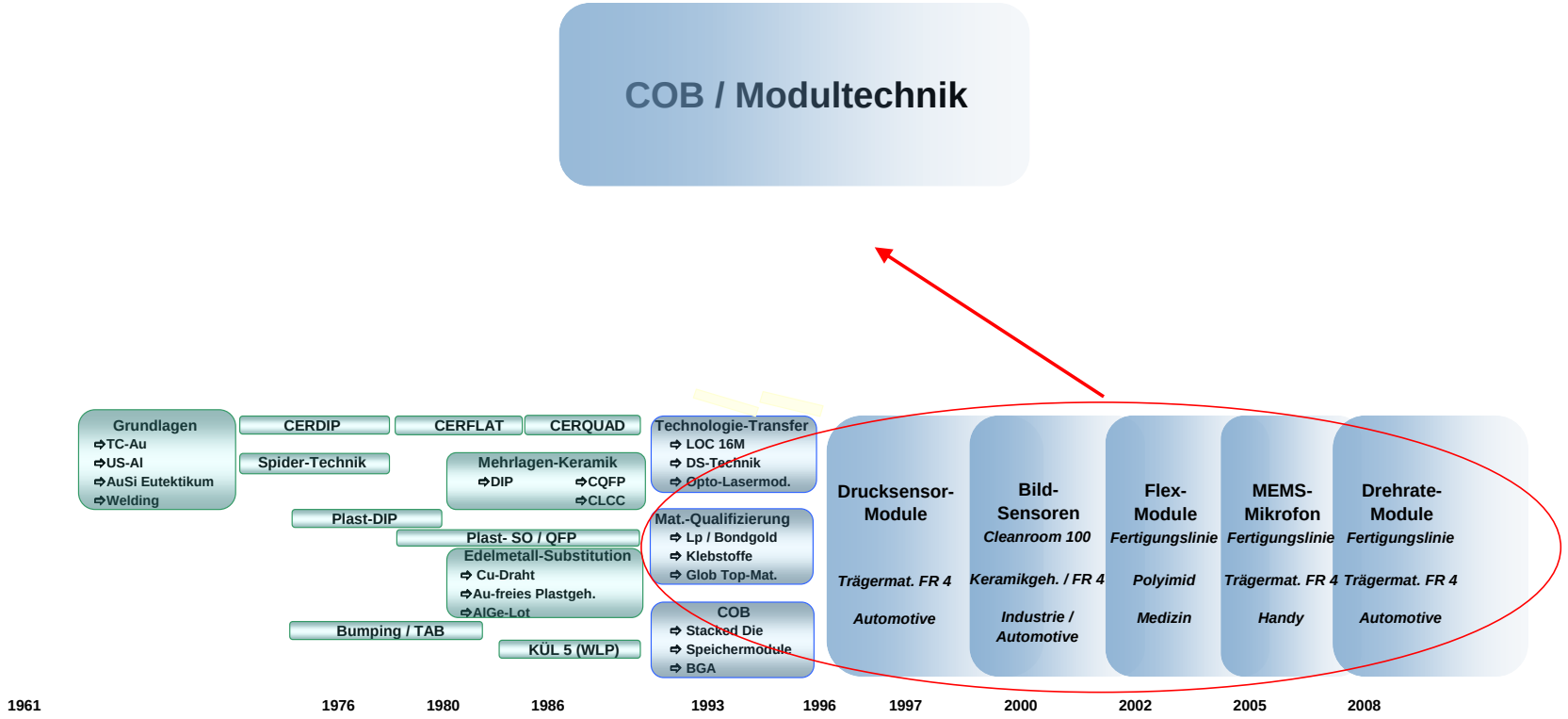
Quelle Qimonda

Alternativen zum Standard Package

⇨ COB tauglich für Massenverfahren

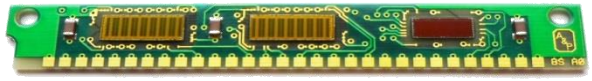
- Anforderungen / Systemuntersuchungen
  - Leiterplatten (PCB) Aufbau u. Materialien
  - Metallisierung (Bondgold)
  - Klebstoffe
  - Abdeckmaterialien (GlobTop)

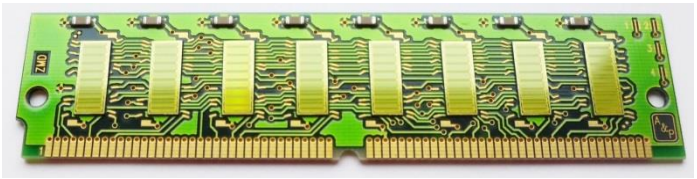
Alternativen zum Standard Package

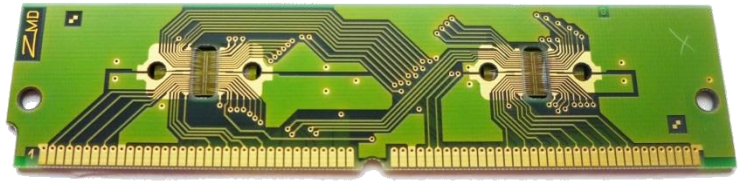


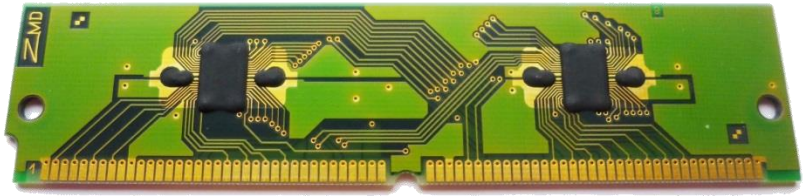
Alternativen zum Standard Package

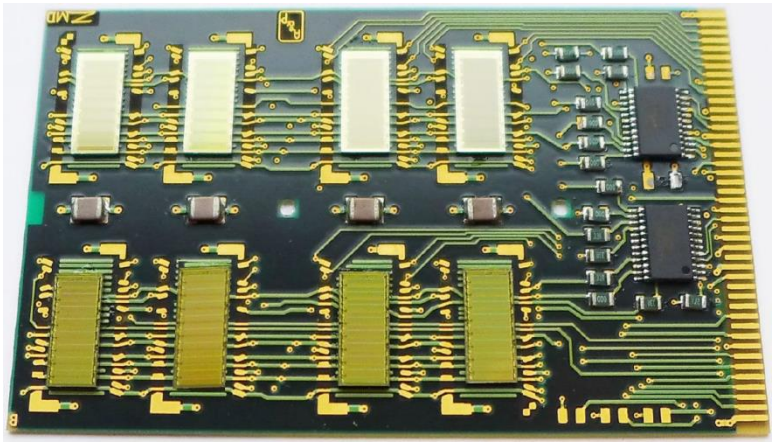
- Speichermodule





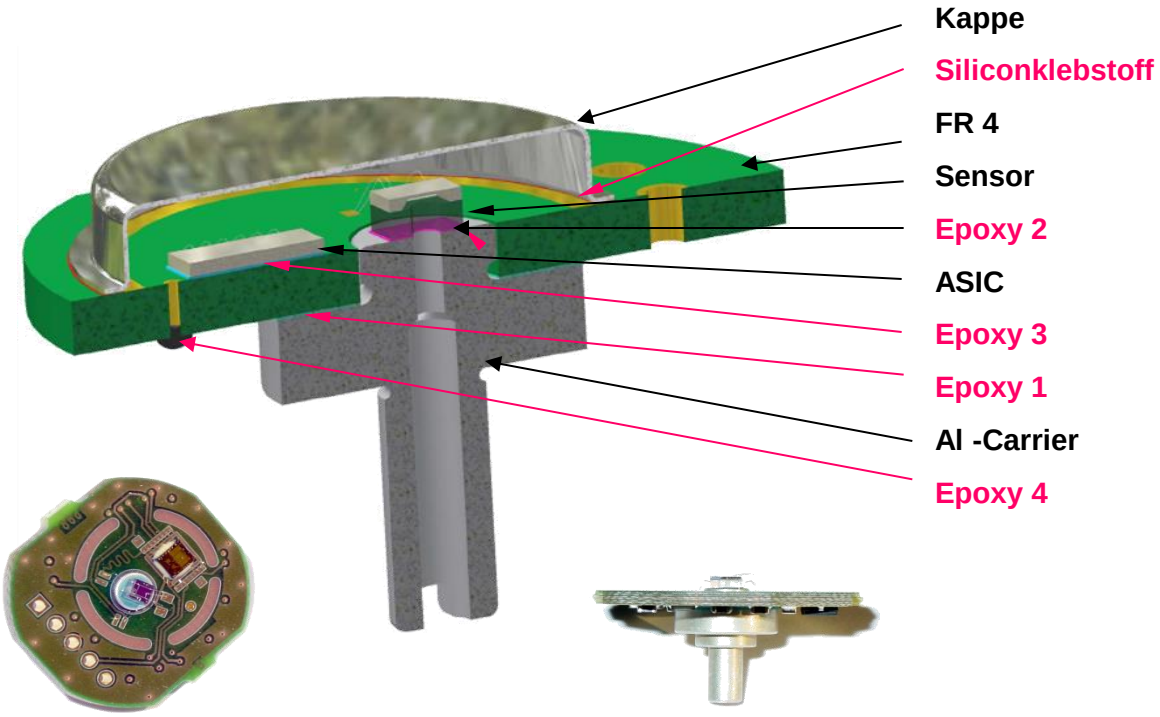


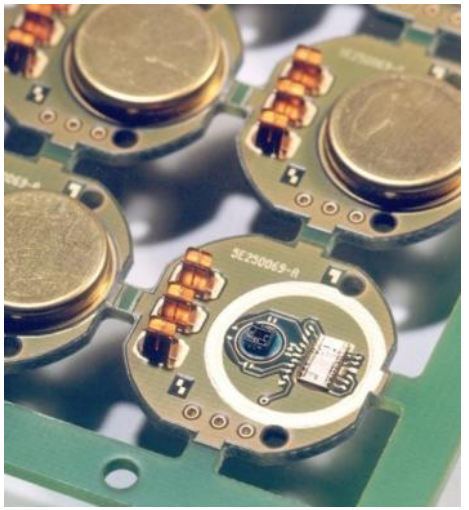




Alternativen zum Standard Package

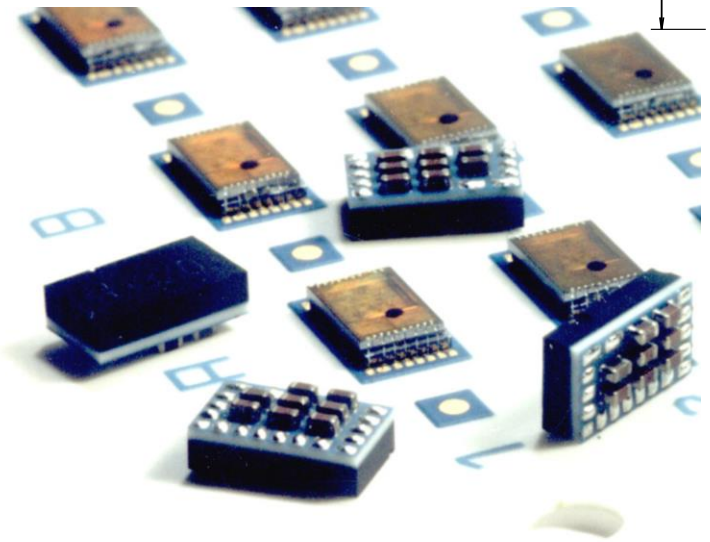
- Drucksensormodul

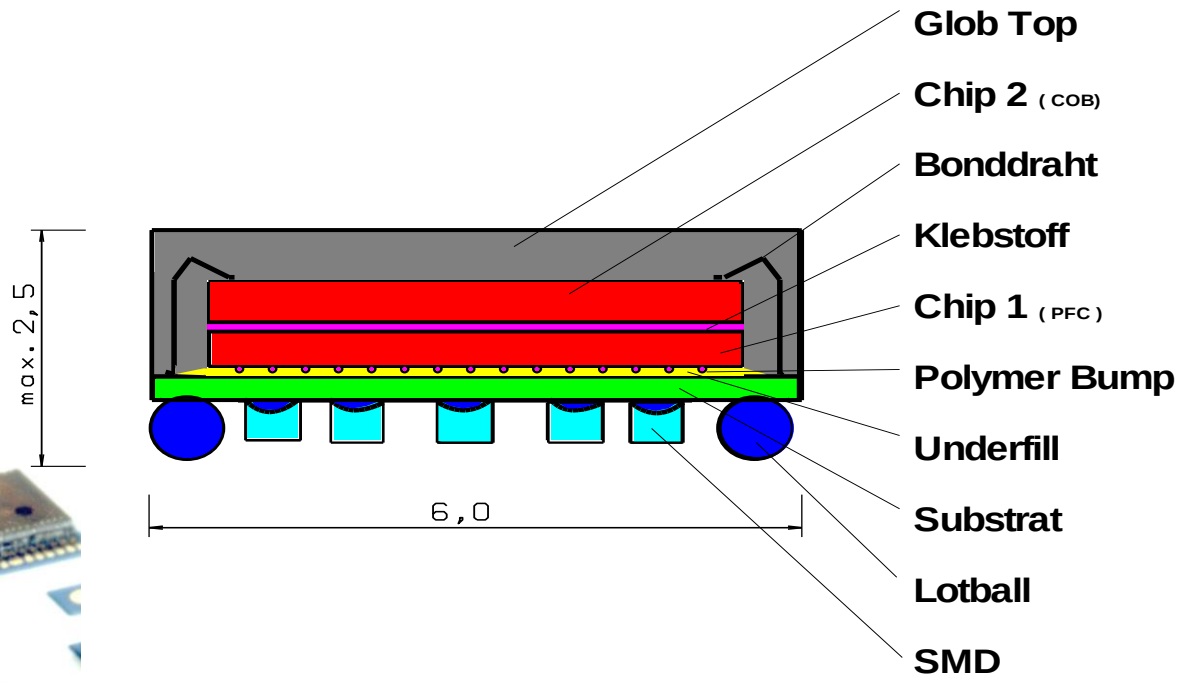




Alternativen zum Standard Package

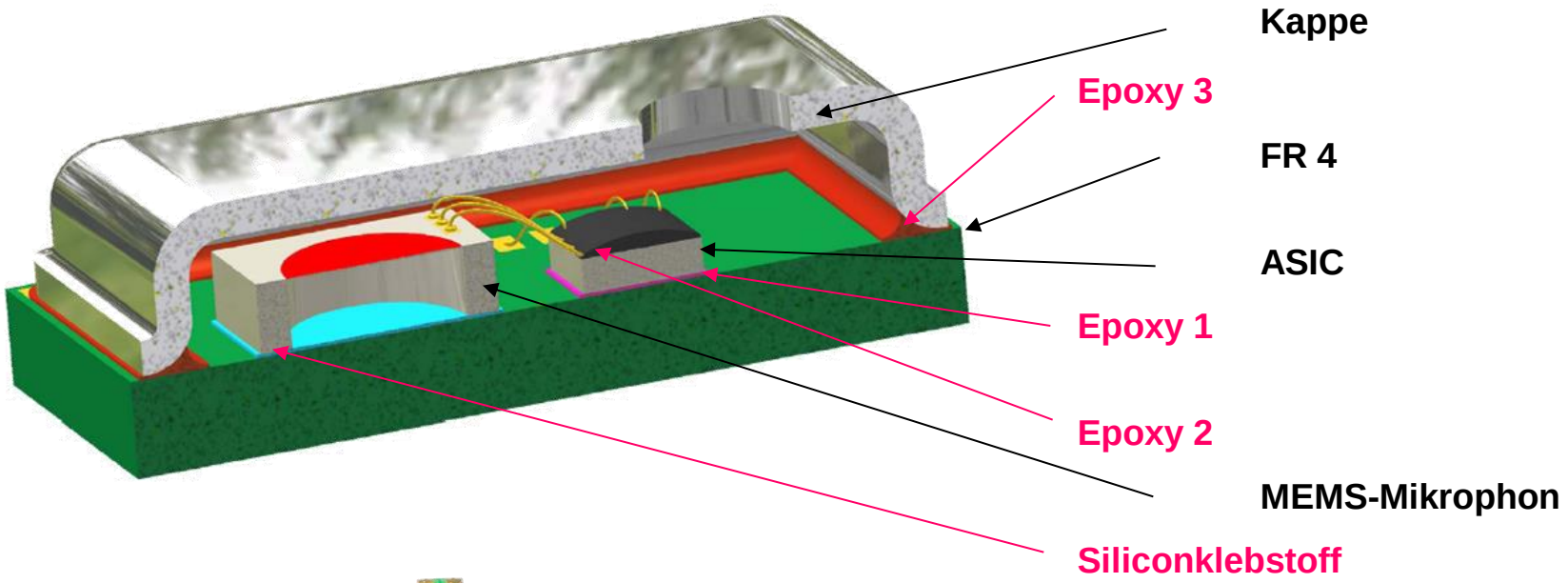
- 3D –Chip Modul

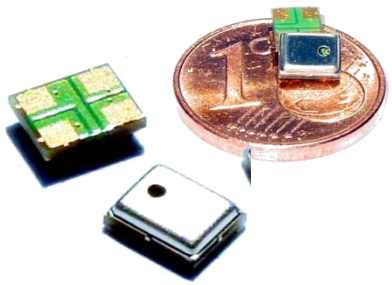




Alternativen zum Standard Package

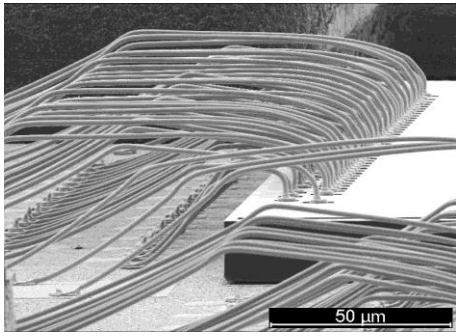
- MEMS Mikrofon

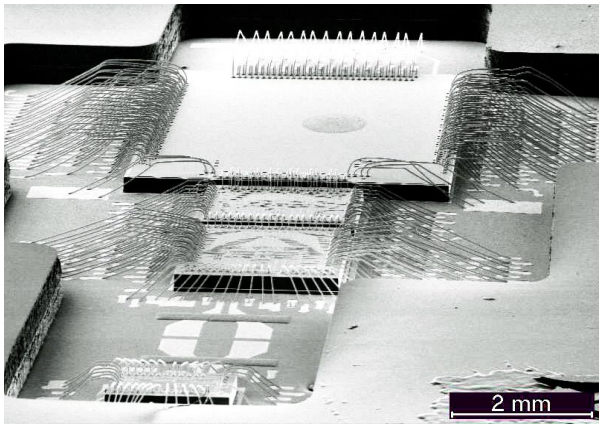


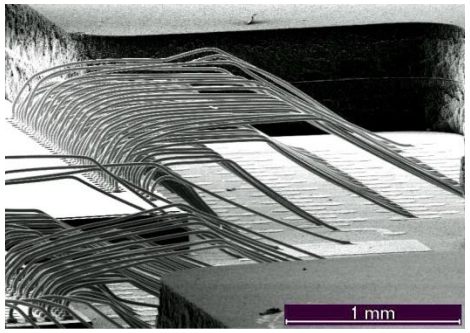


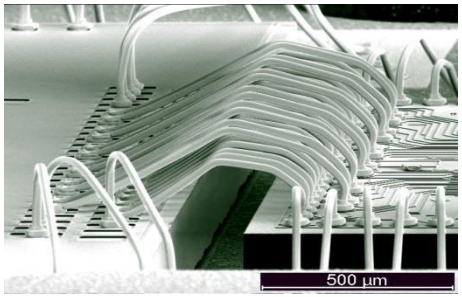
Alternativen zum Standard Package

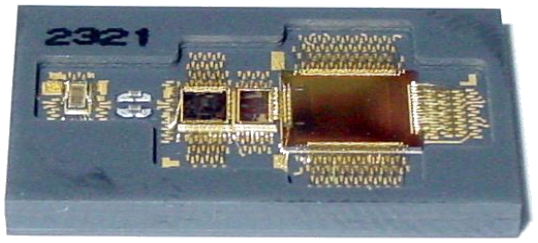
- MCM Module







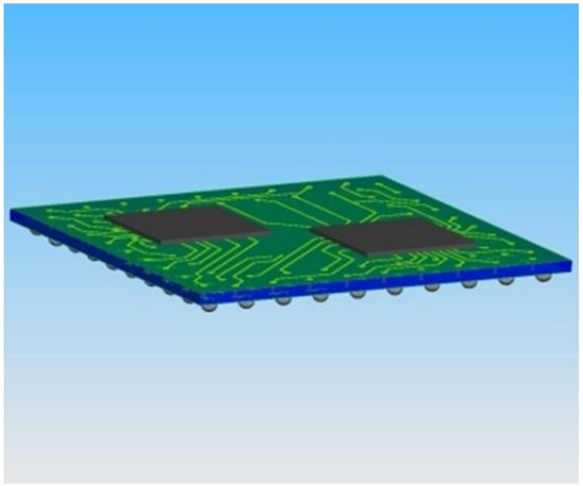




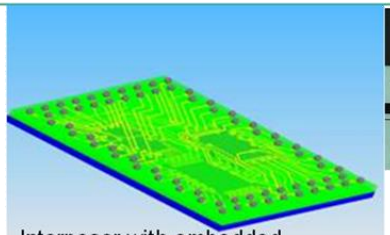
Merkmale: Body:	12 x 21 mm²		Drahtdurchmesser:	Au 30 µm
	Layer:	13 AlN	Anzahl Drahtbonds:	500
	PV $_{max.}$:	20 W	Bondpitch:	50 µ , staggered

Alternativen zum Standard Package

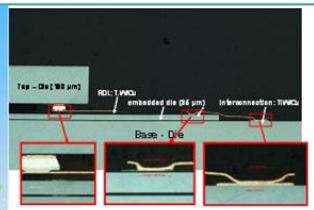
- Systemintegration
  - 3D System Architectures –TSV-Interposer

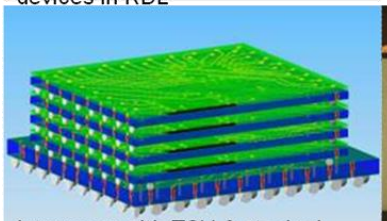


Silicon interposer as device carrier between devices and package / board for high IO count and high interconnect density (multi-layer, 5-10 µm line/space)

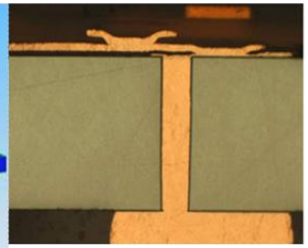


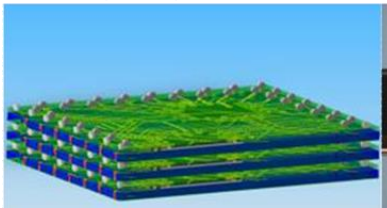
Interposer with embedded devices in RDL



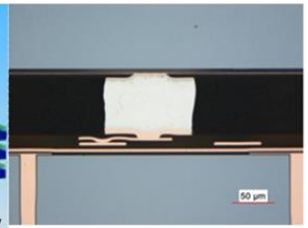


Interposer with TSV & stacked devices (w TSV)



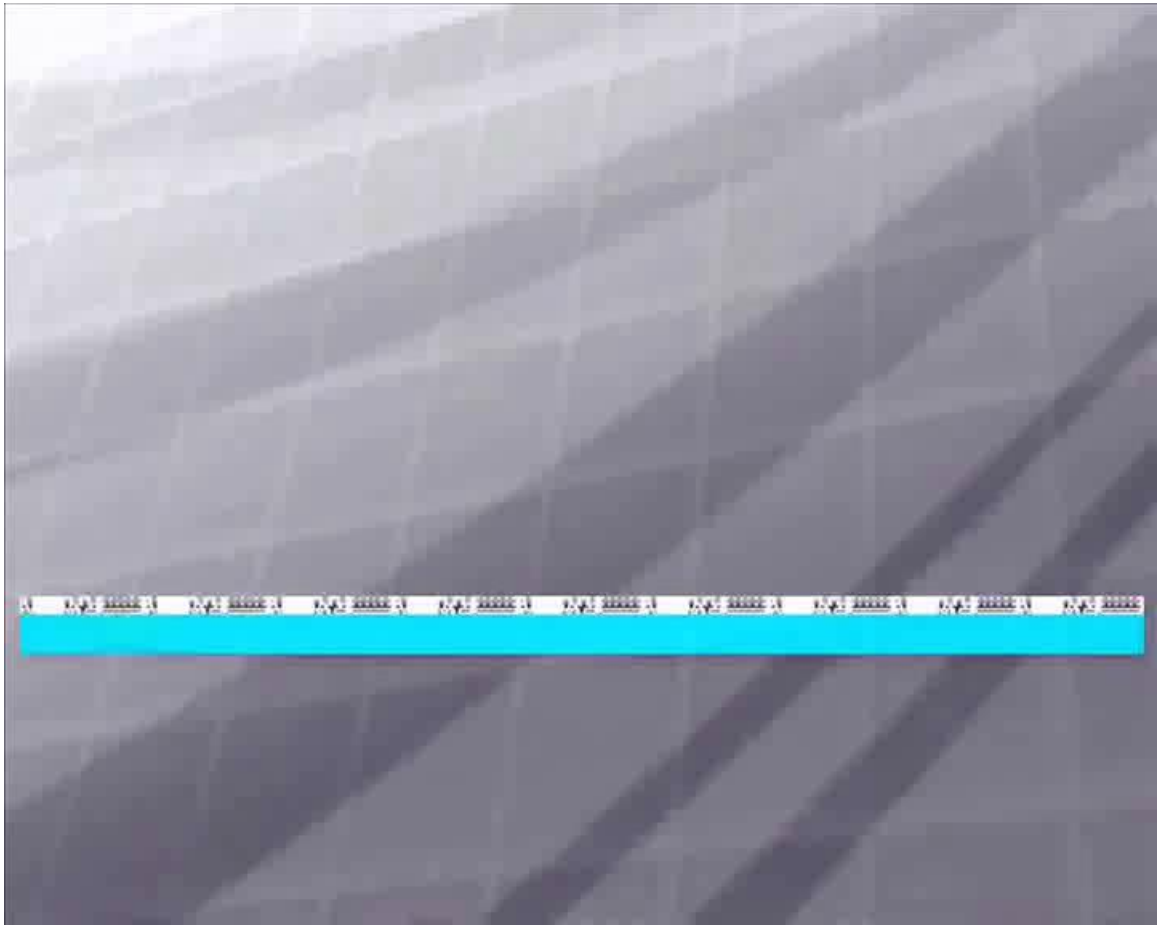


Stacked modular Interposer w. TSV



Alternativen zum Standard Package

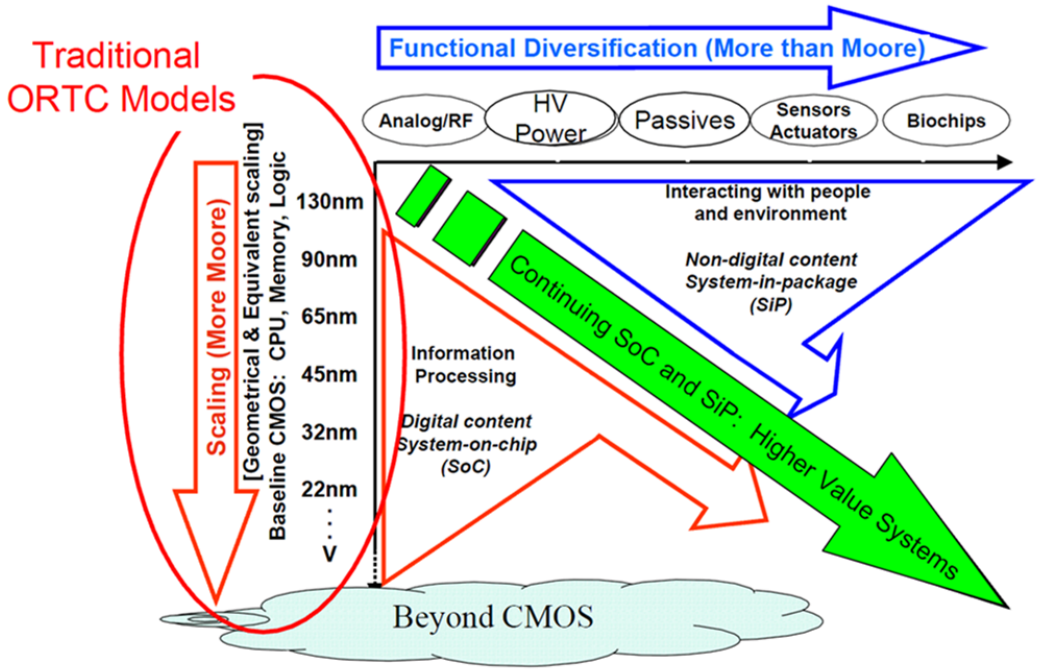
- Systemintegration
  - TSV - Prozess



Alternativen zum Standard Package

- Systemintegration

Motivation for 3D Heterogeneous Integration - SiP



M.J. Wolf

Fraunhofer IZM