Low Temperature Superconductor Electronics

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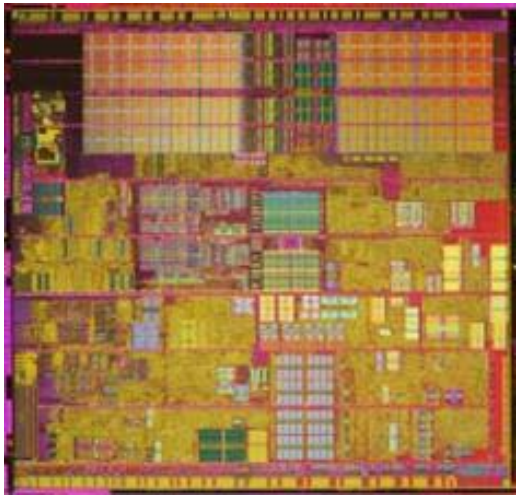
Outline

- Status of Semiconductor Technology
- Introduction to Superconductor Electronics
- Superconductor Electronics Technology
- Applications
- Conclusions

Silicon is not so bad …

Pentium: ~ 100mm^2×5µm active layer = 0.5mm^3



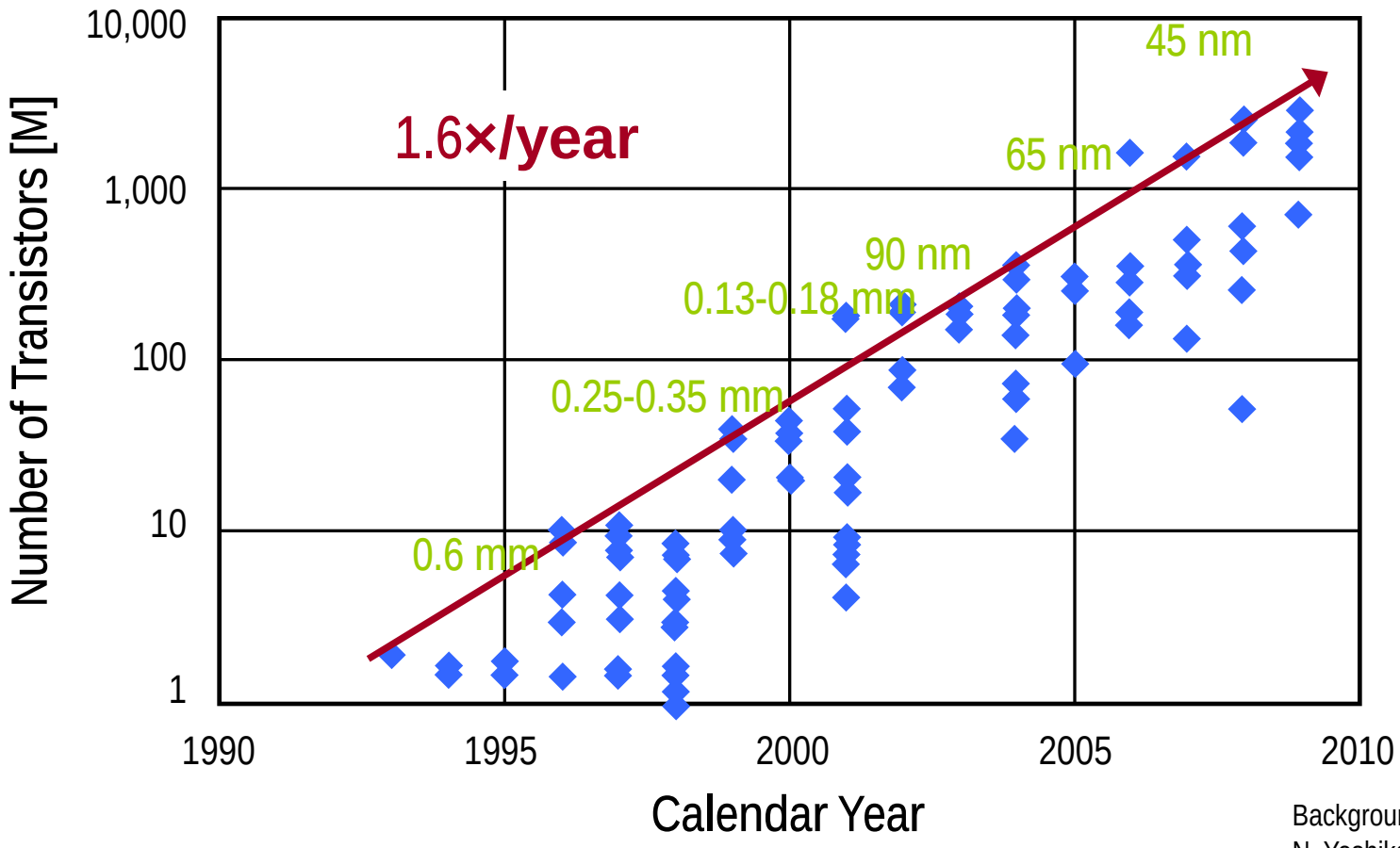
Mosquito's head ~ 0.5mm^3 ?

Computers are capable of …

- wining chess with Gary Kasparov (Deeper Blue > 1,000×Pentium)
- Forecasting next day's weather
- calculating trajectory of Mars
- making my slides

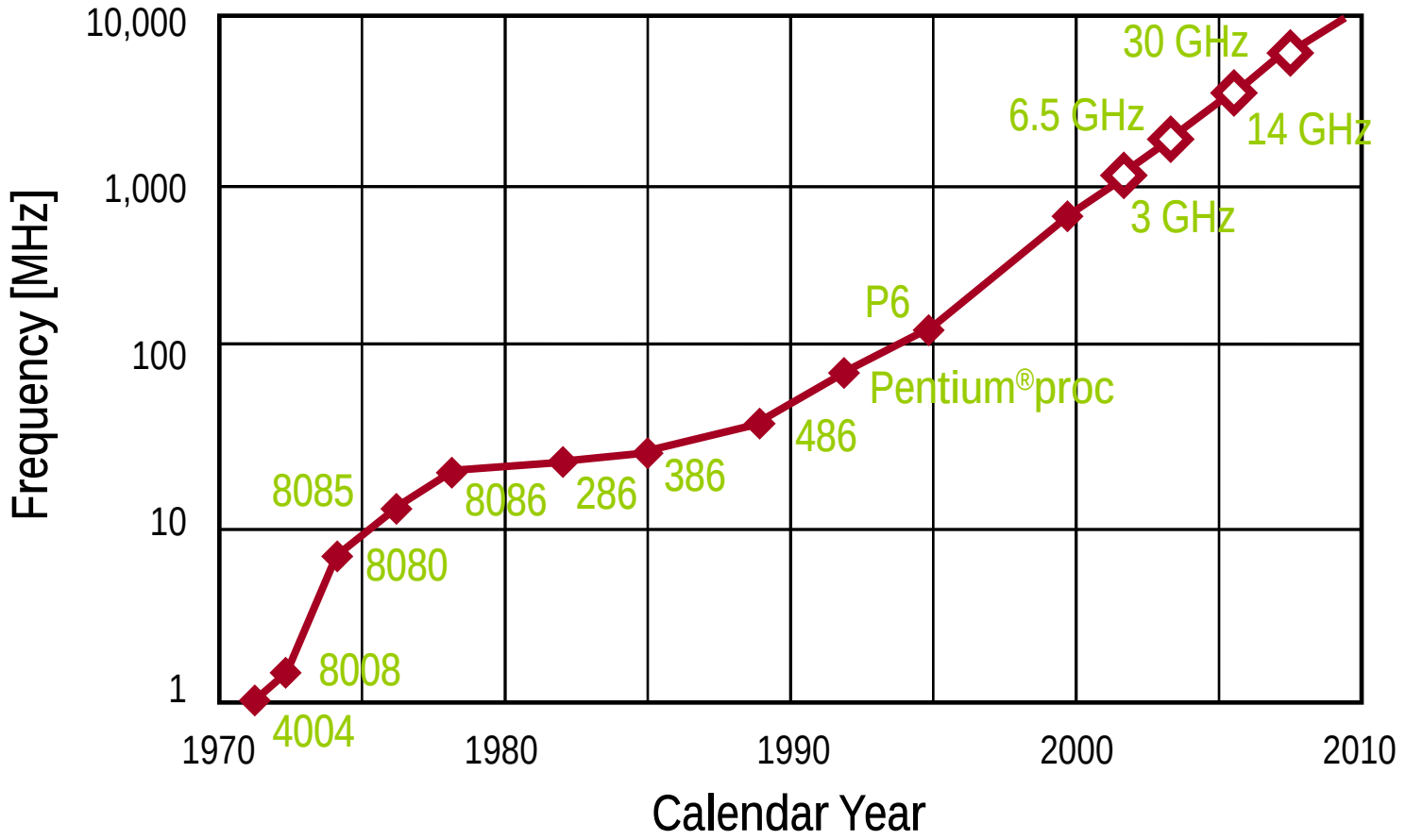
Moore's Law - Chip Complexity

Trends of the number of transistors on a single chip of recent high performance processors



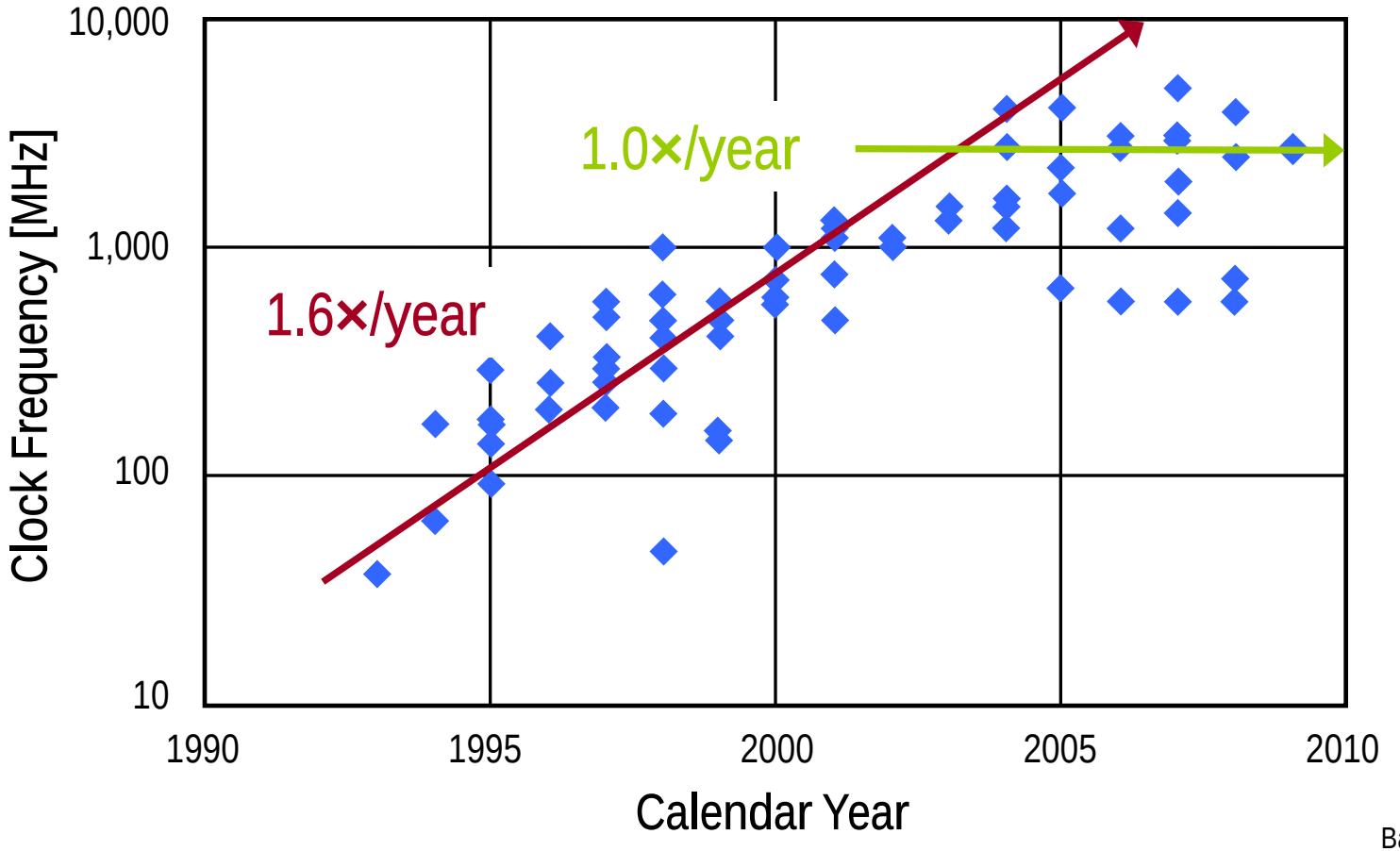
Background slide from
N. Yoshikawa

Consequences of Scaling - Clock Frequency



Breakdown of Moore's Law for Clock Frequency

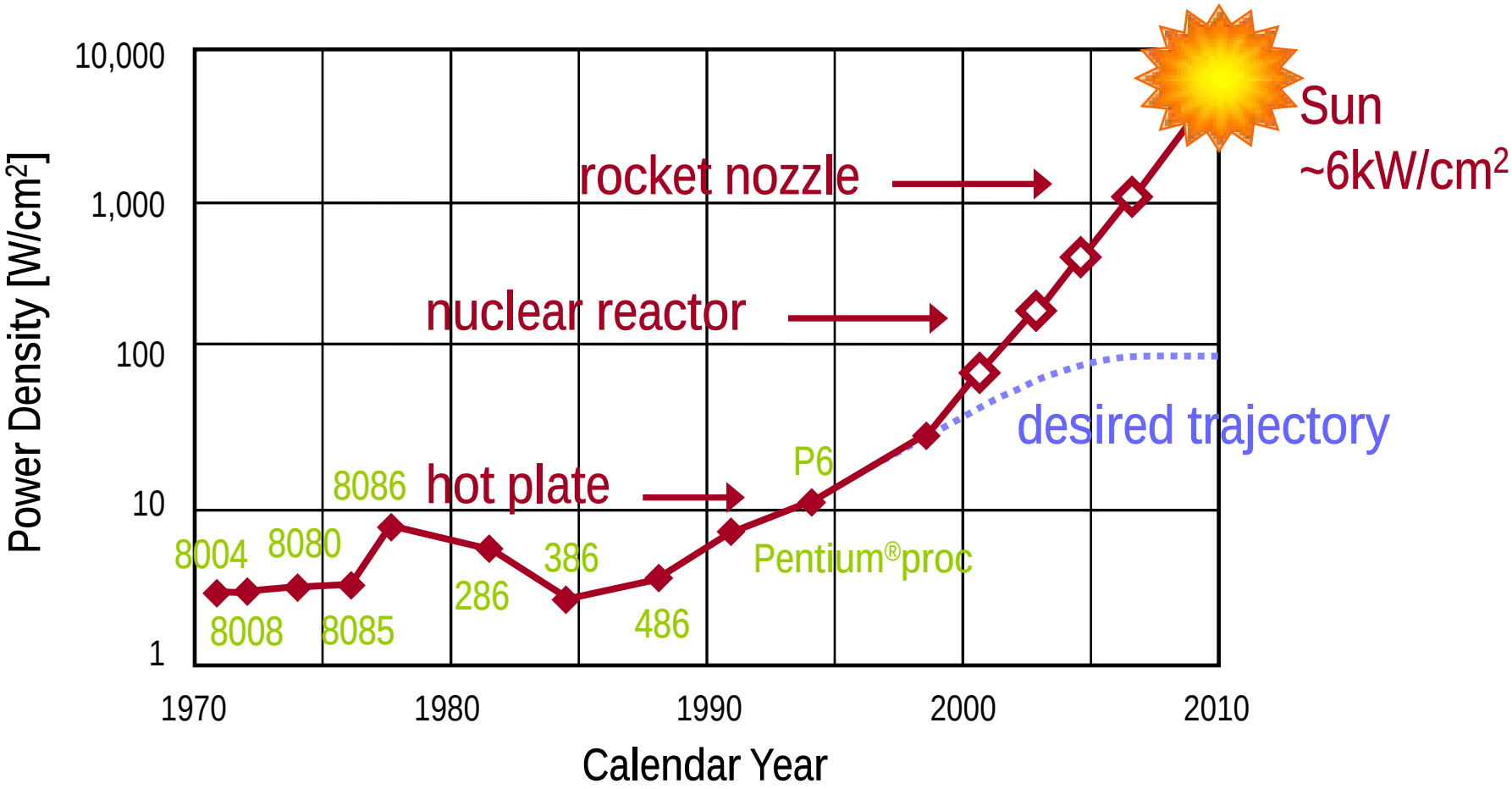
Trends of the clock frequency of recent high performance processors



Background slide from
N. Yoshikawa

Power Density Will Increase

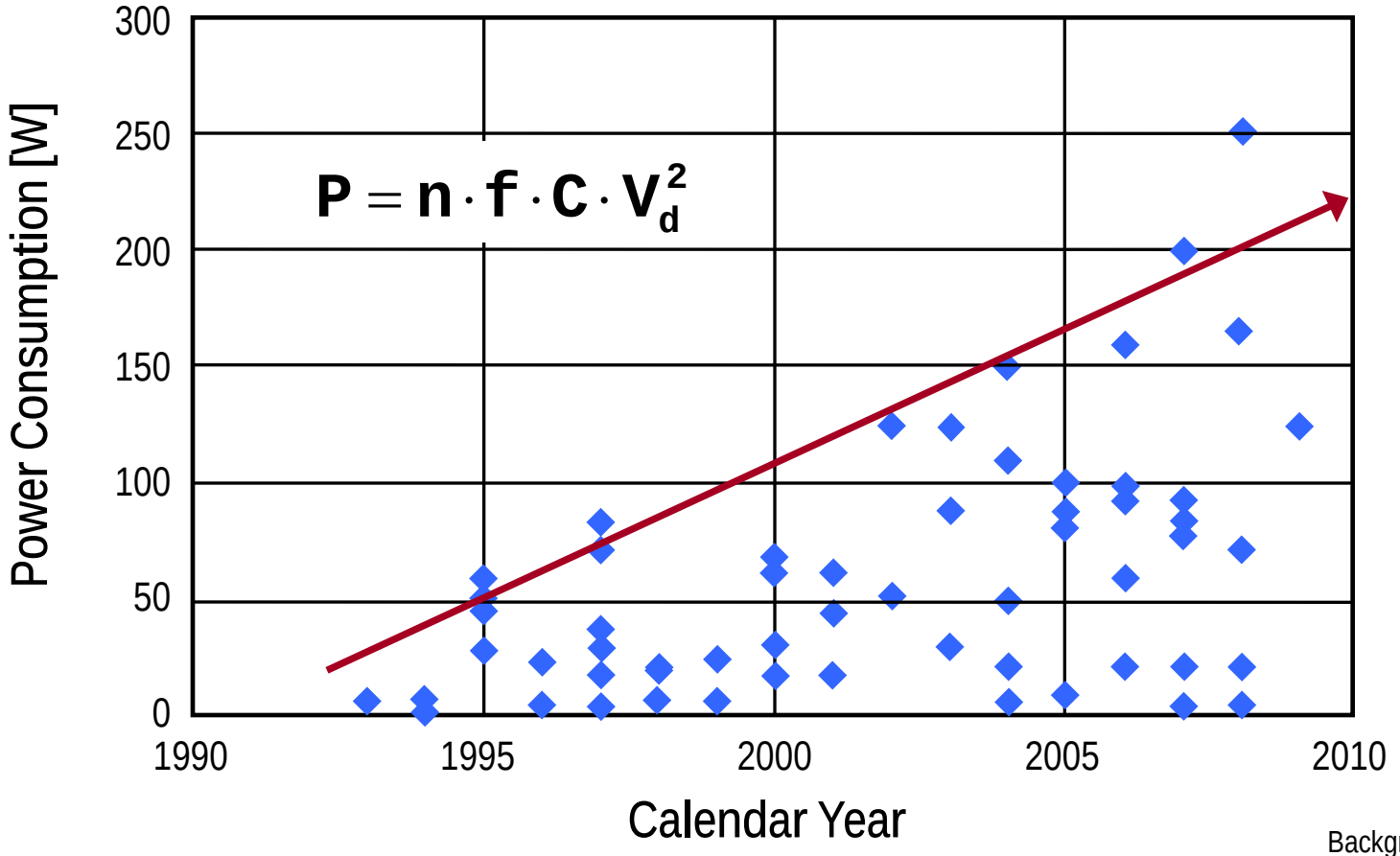
$$P = n \cdot f_{requency} \cdot C_{load} \cdot V_d^2$$



Ref. Intel

Increase of Power Consumption

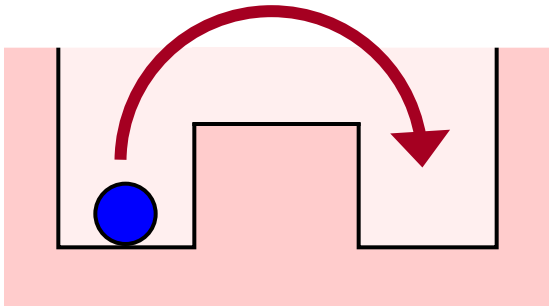
Trends of the power consumption of single chips of recent high performance processors



Background slide from N. Yoshikawa

Limit Technology - Lowest Barrier

Double potential well:
thermal escape



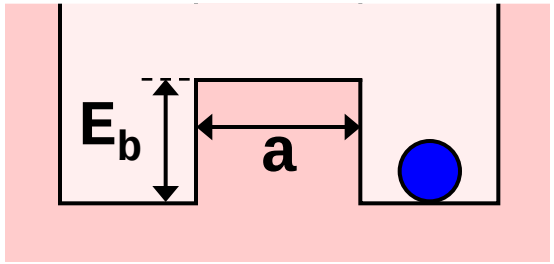
Required:

low probability Π of spontaneous thermal transitions between two wells (error probability)

$$\Pi_{classic} = \exp\left(-\frac{E_b}{k_B T}\right)$$

Limit:

$$\frac{1}{2} = \exp\left(-\frac{E_b}{k_B T}\right) \quad \rightarrow \quad E_b = k_B T \cdot \ln 2$$



Ref. R. Cavin, V. Zhirnov,
J. Hutchby & G. Burianoff, SCR

Limit Technology - Heisenberg's Uncertainty Principle

- Minimum size x_{min} of a switch (Heisenberg uncertainty principle):

$$x_{min} = \frac{\hbar}{\Delta p} = \frac{\hbar}{\sqrt{2 m_e E_{bit}}} = \frac{\hbar}{\sqrt{2 m_e k_B T \ln 2}} = 1.5\text{nm } (T = 300\text{K})$$

- Minimum size corresponds to a maximum integration density n_{max} of switches:

$$n_{max} = \frac{1}{x_{min}^2} = 4.7 \cdot 10^{13} \text{switches/cm}^2 \quad \text{ITRS22nm node: } 2.2 \cdot 10^9/\text{cm}^2$$

- Minimum switching time τ_{min} (Heisenberg uncertainty principle):

$$\tau_{min} = \frac{\hbar}{\Delta E} = \frac{\hbar}{k_B T \ln 2} = 0.04\text{ps} \quad \text{ITRS22nm node: } 0.15\text{ps}$$

- Power dissipation P of this limit technology:

$$P = \frac{n_{max} \cdot E_{bit}}{\tau_{min}} = 3.7 \cdot 10^6 \text{W/cm}^2 \text{ ultimate!}$$

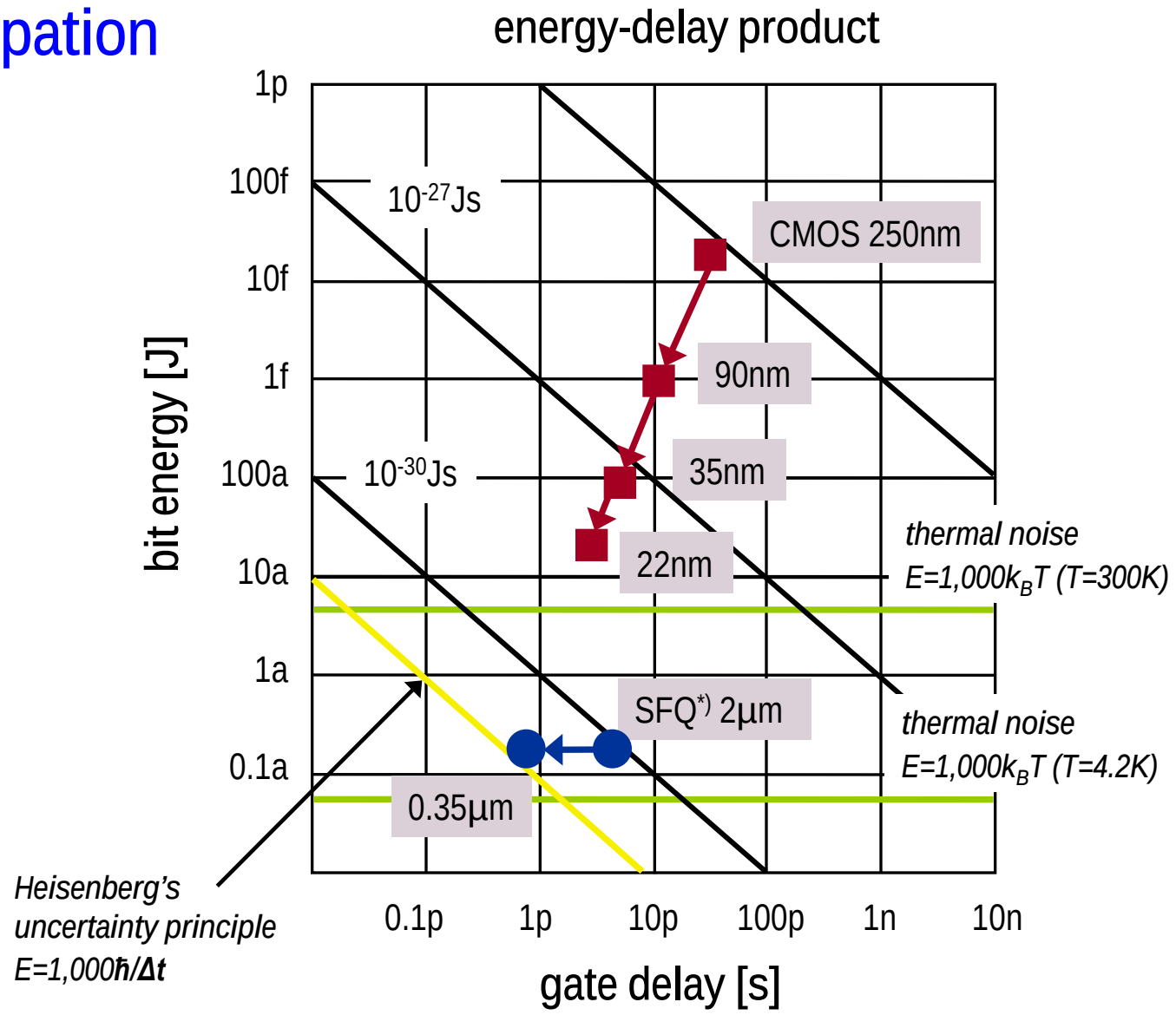
ITRS22nm node: 100W/cm² practical

Ref. A. Jakubowski, A. Swit

End of Story?

Use Magnetic Flux Quanta
Instead of
Electrical Charges

Power Dissipation



*) Single Flux Quantum

Single Flux Quantum Electronics

Basic building blocks of SFQ circuits

- Josephson Junction: basic switching device, generates single flux quanta
- Inductance
- Resistor

In contrast to CMOS

In SFQ circuits inductances define the functionality.

The mode of operation depends on the wiring between the Josephson junctions.

Drawbacks

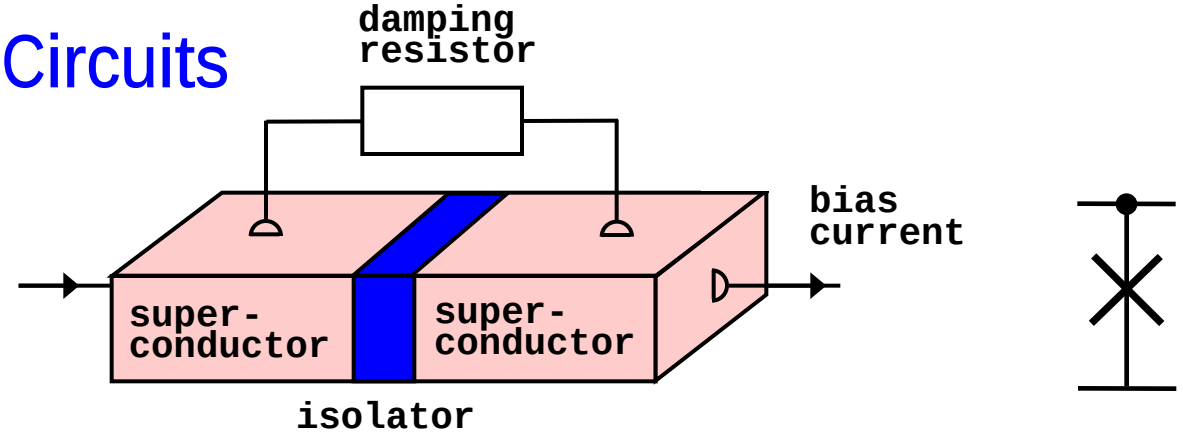
- Careful inductance calculation is required.
- Layout scaling is not possible.
- Storage of flux quanta is chip-area-consuming.

Important Attributes of SFQ Digital Circuits

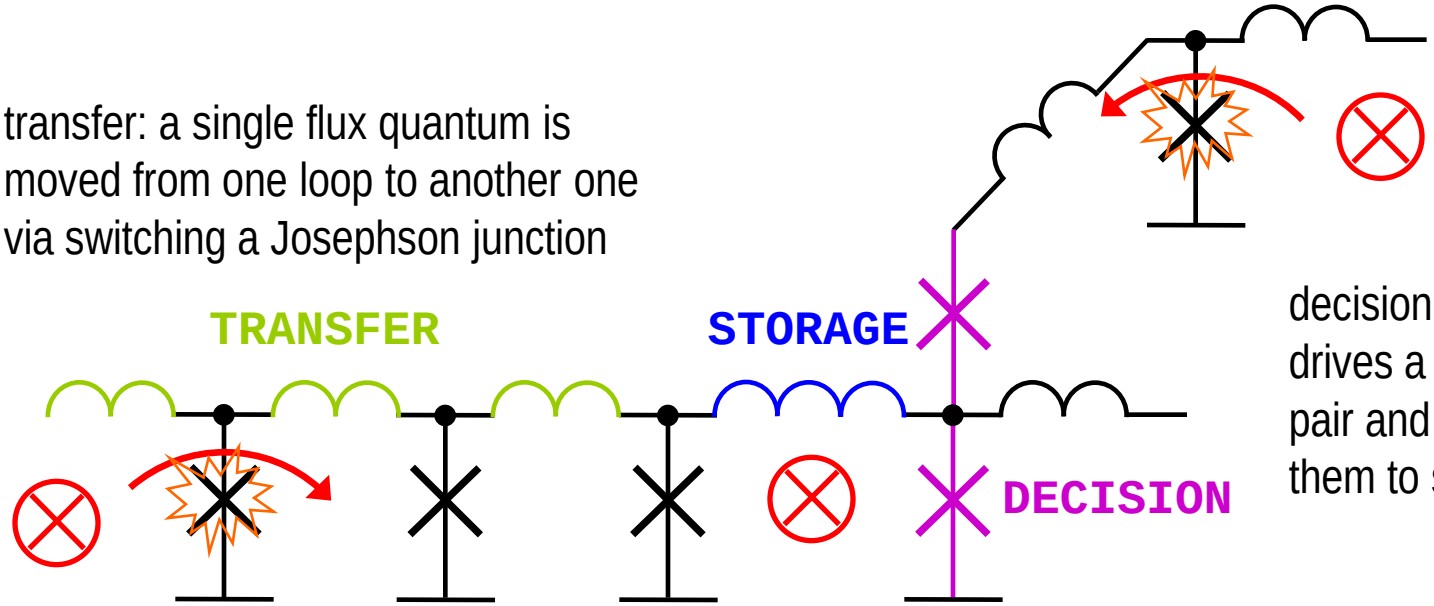
- Fast and low-power switching devices that generate identical single-flux-quantum data pulses.
- Loss-less superconducting wiring for power distribution.
- Latches that store a magnetic-flux quantum.
- Low loss, low dispersion integrated superconducting transmission lines that support “ballistic” data and clock transfer at the clock rate.
- Cryogenic operating temperatures that reduce thermal noise and enable low power operation.
- SFQ circuit fabrication that can leverage processing technology and computer-aided design (CAD) tools developed for the semiconductor industry.

Operation of SFQ Circuits

SFQ circuits are built from superconducting loops and overdamped Josephson junctions



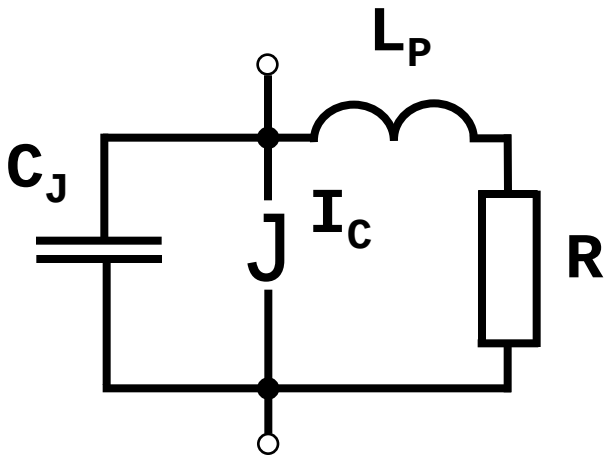
transfer: a single flux quantum is moved from one loop to another one via switching a Josephson junction



decision: a clock signal drives a tow junction pair and forces one of them to switch

storage: a large inductor allows to store the circulating current and traps the flux quantum

Josephson Junction Characteristic Parameters



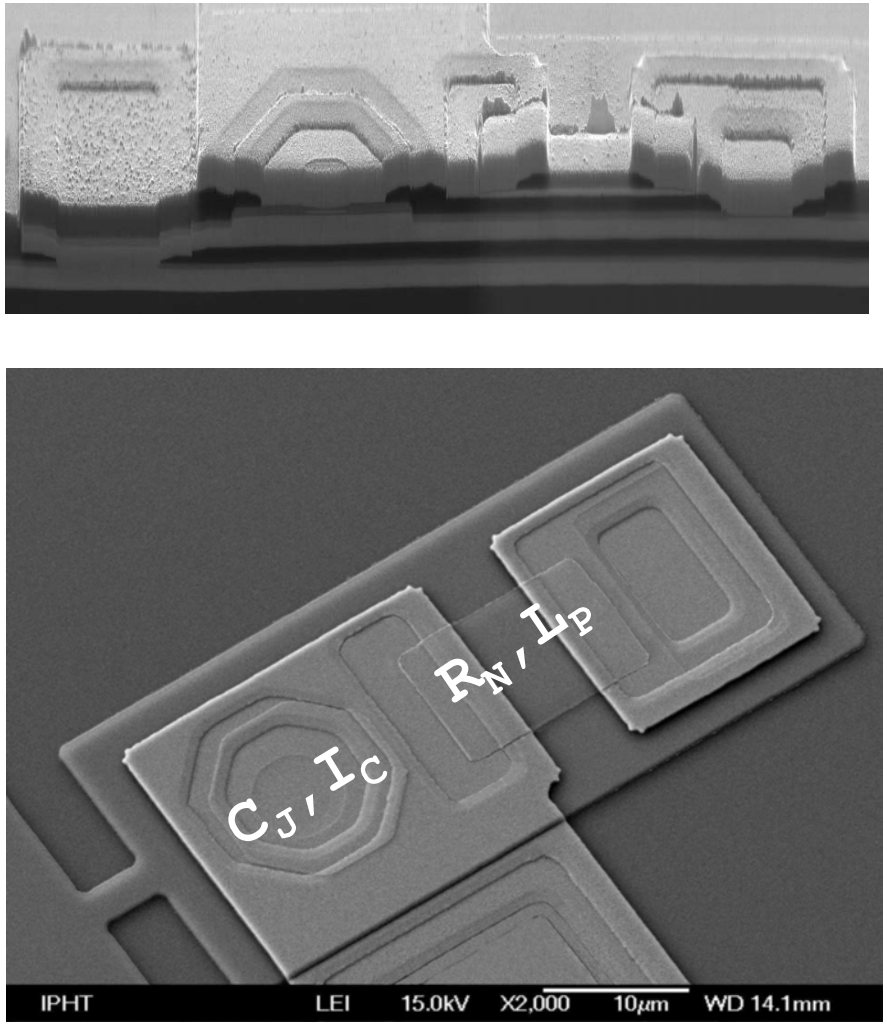
critical current density $j_C = 1 kA/cm^2$

critical current $I_C = 250 \mu A$

capacitance $C_J = 1.25 pF$

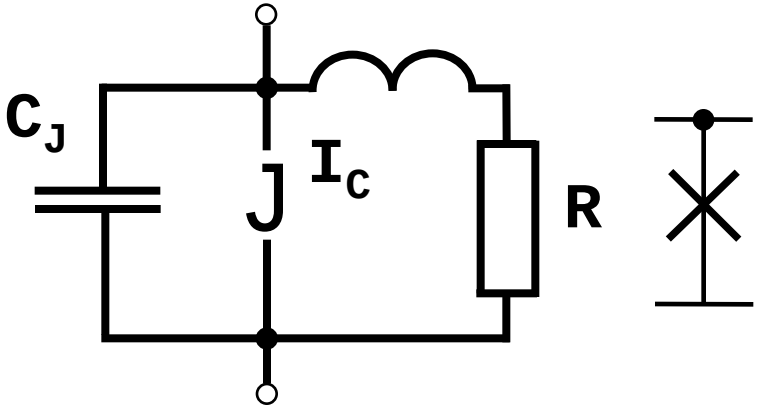
resistance $R \sim 1\ \Omega$

parasitic inductance $L_P = 1 pH$

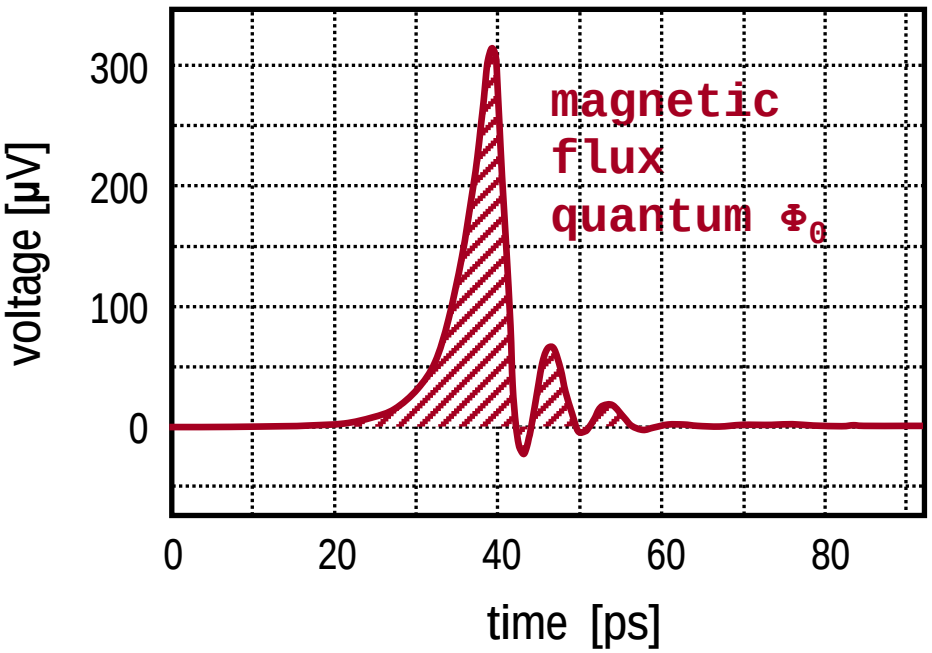


Josephson junction as a thin-film device. Cross section and top view.

Josephson Junction Dynamics



$$\Delta\Phi = \int V(t)dt = \Phi_0 = \frac{h}{2e} = 2.07\,\mathrm{mV}\cdot\mathrm{ps}$$



pulse duration $\tau_{SFQ} = \frac{\pi}{\omega_C} \cong 1\,\mathrm{ps}$

pulse amplitude $V_{max} = 2I_C R \cong 1\,\mathrm{mV}$

energy $E = I_C \Phi_0 \cong 2\cdot 10^{-19}\,\mathrm{J}$

dissipated power $P_D = 2I_C^2 R \cong 0.1\,\mu\mathrm{W}$

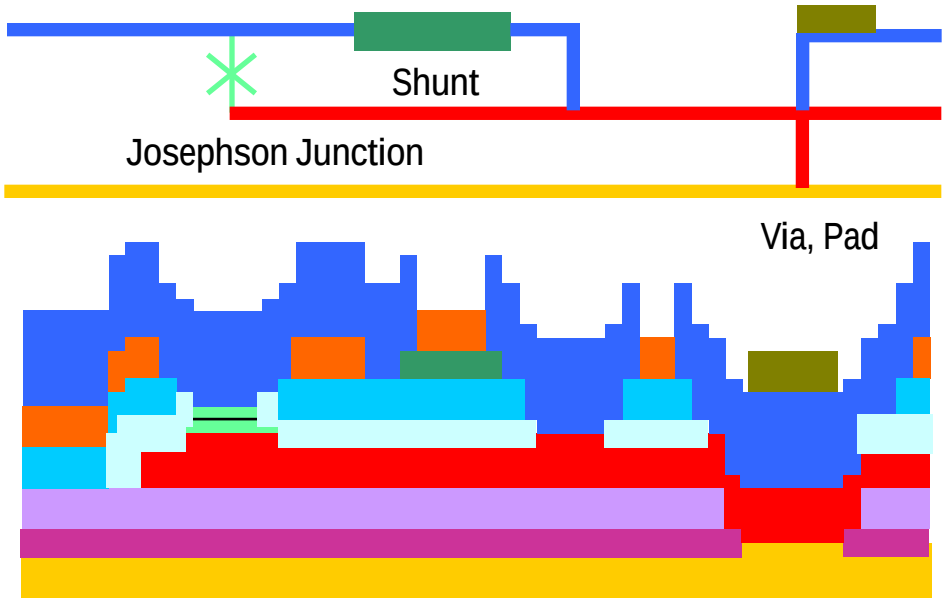
char. frequency $\omega_C = \frac{2\pi I_C R}{\Phi_0} \rightarrow f_C = 500\,\mathrm{GHz}$

SFQ pulse at a Josephson junction with I_C = 250μA, R = 1.02Ω, C = 1.26pF, and $I_C R$ = 0.255mV; pulse width ~ 6.5ps, pulse amplitude ~ 320μV.

Superconductor Electronics Technology

Main features of SFQ technology

- Works with metals rather than semiconductors
- Three superconducting layers
- Nb/AlAlO$_X$/Nb trilayer for junctions with typically j_C=1 kA/cm^2
- External shunt with typical sheet resistance of 1Ω/□



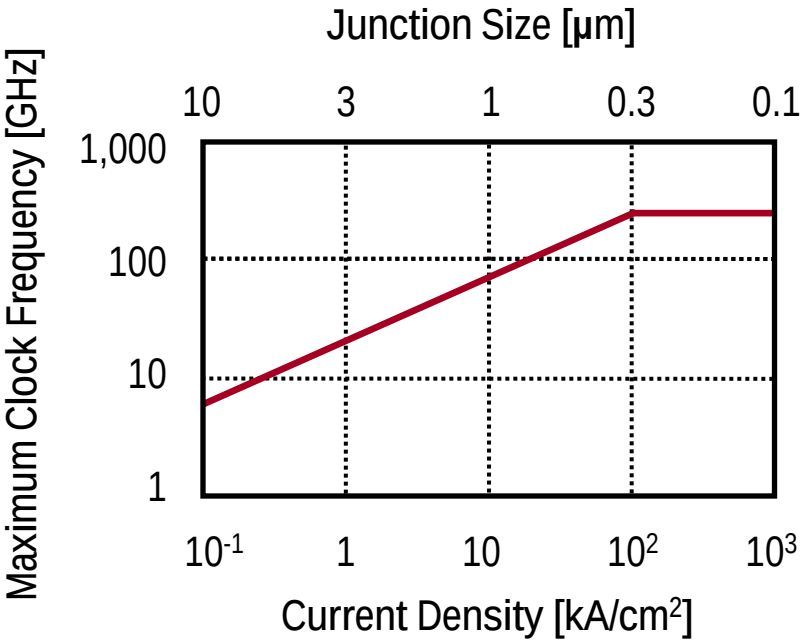
Layer	Thickness	Material
R2	50 nm	Au
M2	350 nm	Nb
I2	150 nm	SiO
R1	80 nm	Mo
I1B	150 nm	SiO
I1A	70 nm	Nb_2O_5
T1	60 nm 12 nm 30 nm	Nb Al_2O_3 Nb
M1	250 nm	Nb
I0B	200 nm	SiO
I0A	50 nm	Nb_2O_5
M0	200 nm	Nb

Scaling Down SFQ - Chip Performance

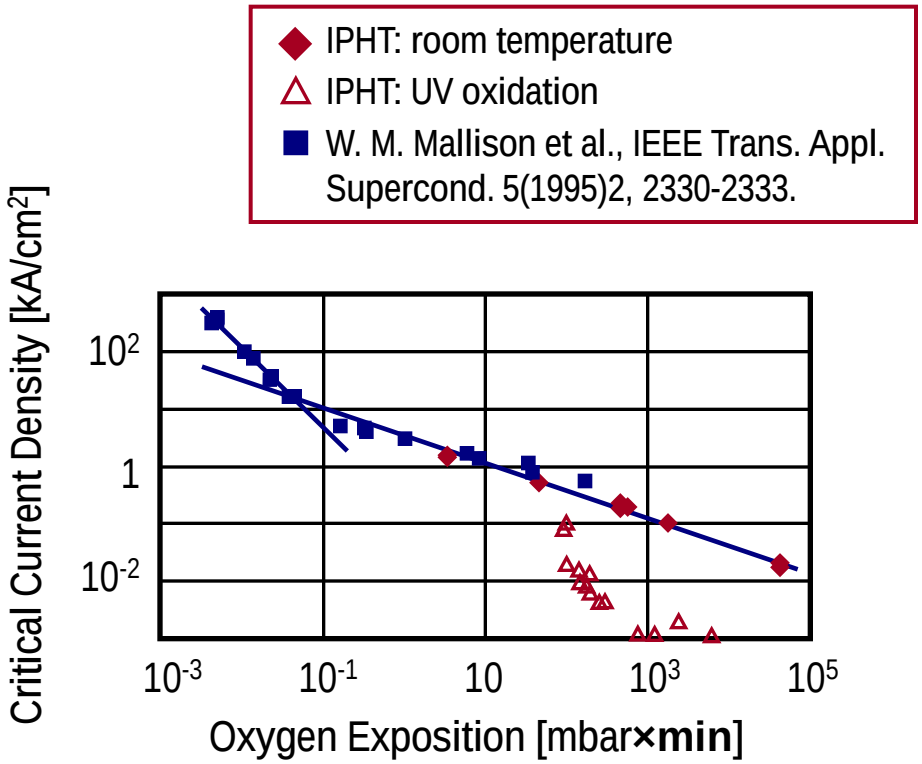
Josephson Junction Size [µm]	Integrated Circuit Density [cells per cm²]	Integration Level	SFQ Pulse Width [ps]	Maximum Clock Rate [GHz]	Minimum Power Dissipation [µW per cell]
3.5	10,000	LSI	4	10-40	0.03
1.5	30,000	VLSI	2	40-80	0.06
0.8	100,000	ULSI	1	70-130	0.1
0.4	1,000,000	SLSI	0.8(?)	100-200(?)	0.15(?)

Basic figures of merit for niobium trilayer SFQ circuits for different minimum feature sizes.

Scaling down the SFQ - Technology



Shrinking superconductor electronics. Scaling the junction size down to 0.3 µm the clock speed of integrated circuits can be increased well-above 100 GHz.



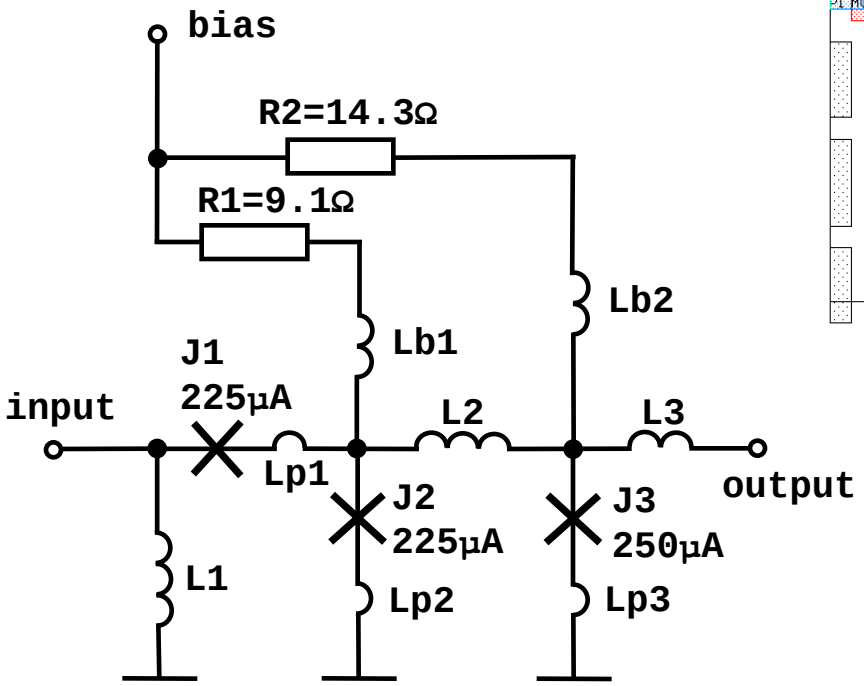
Critical current density as a function of oxygen exposition; ultra-violet light-assisted oxidation allows to reach very low values of the critical current density (triangles).

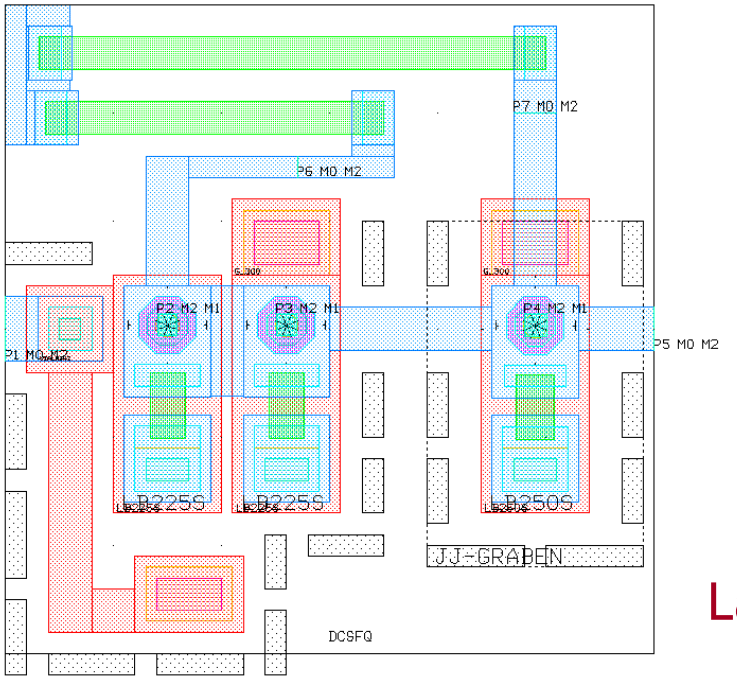
SFQ Foundries

	Japan		USA		EU
Institution	NEC		Hypres		IPHT
Process	SDP	ADP2	1000-1	4500-1	rsfq1d
Current Density [kA/cm^2]	2.5	10	1	4.5	1
Minimum Lateral JJ Dimension [µm]	2	1	3	1.5	3.5
Nb Layers	3	6 …10	4	4	3
Complexity		23.5k		12k ...15k	5k

Manufacturing facilities for niobium-based digital superconducting electronic circuits on costumer request.

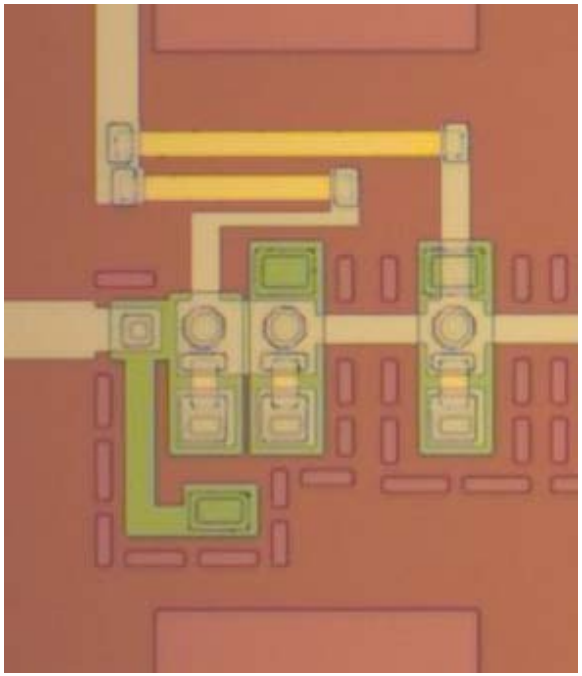
dc-SFQ Converter





Layout

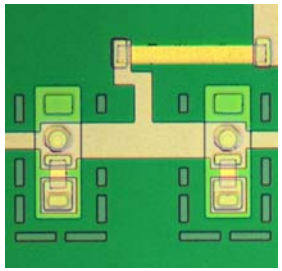
Chip



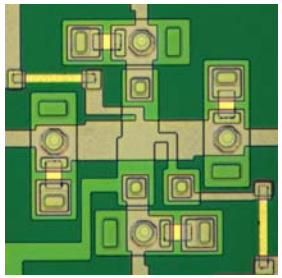
Schematic. The optimisation of parameters is very important for the correct function.

Standard Cell Library

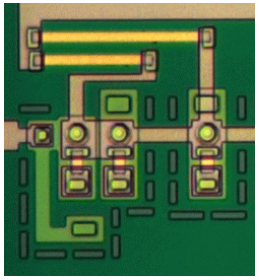
www.fluxonics-foundry.de



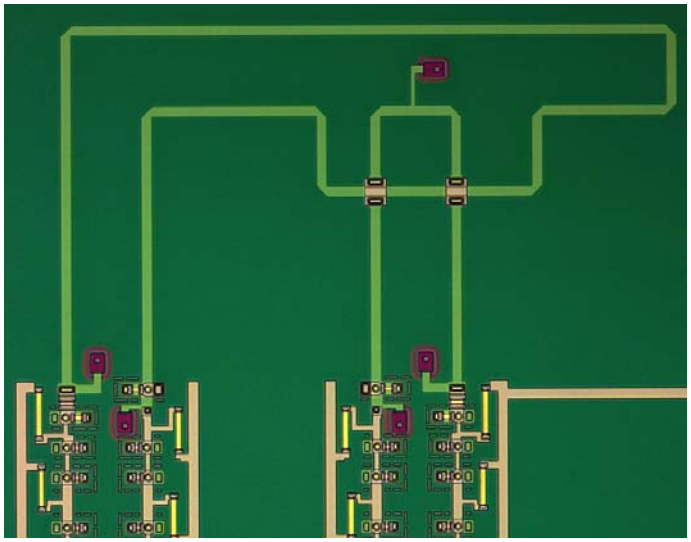
Josephson transmission line



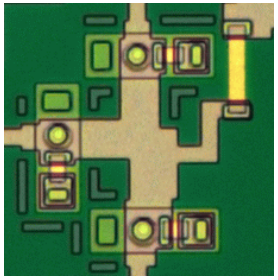
Line Crossing



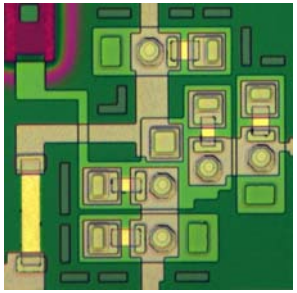
dc/SFQ converter



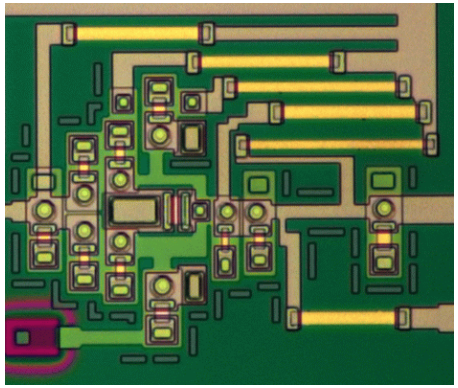
micro-strip line interconnects (MSL)



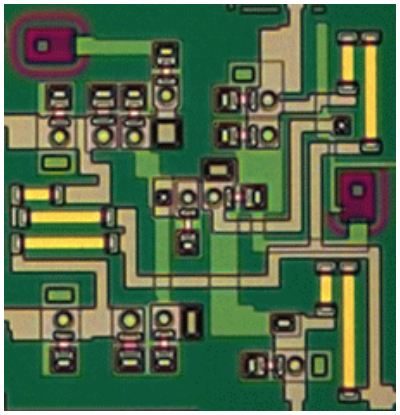
splitter



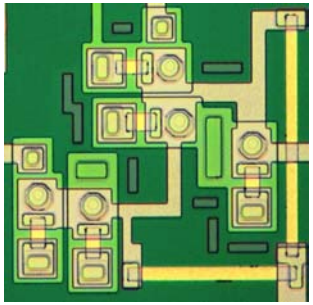
merger



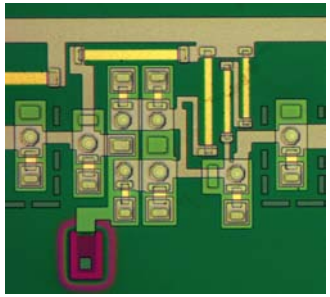
SFQ/dc converter



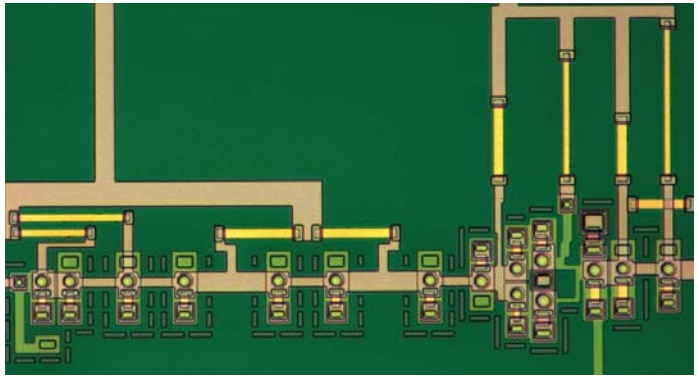
RS-FF



delay-FF



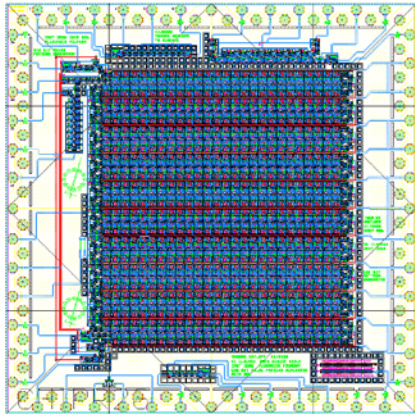
toggle-FF



dc/SFQ-JTL-SFQ/dc circuit

Circular Shift Register

www.fluxonics-foundry.de



512 bit memory

5,153 Josephson junctions

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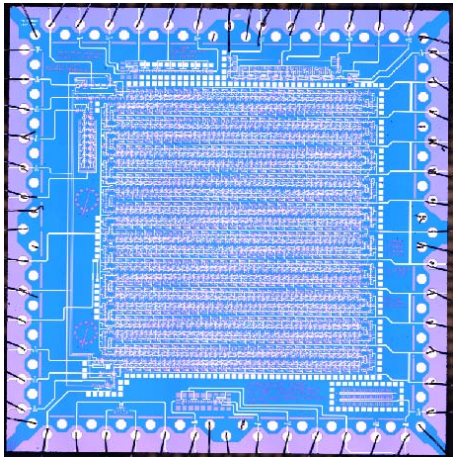
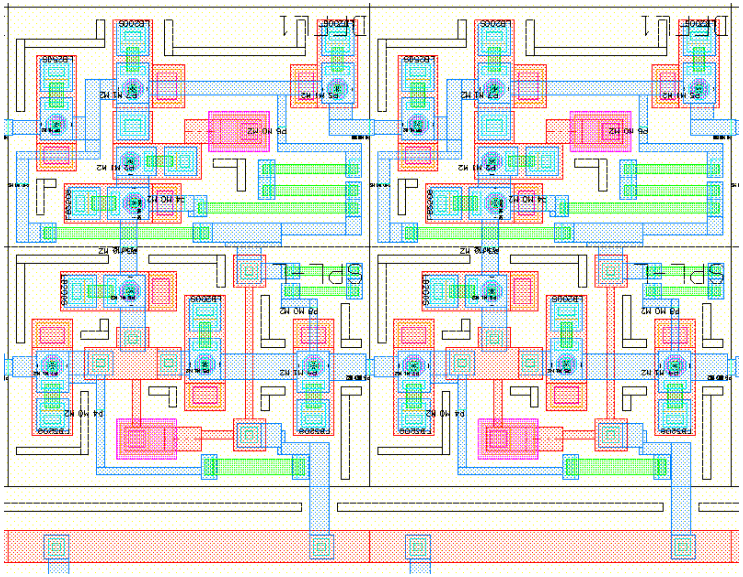
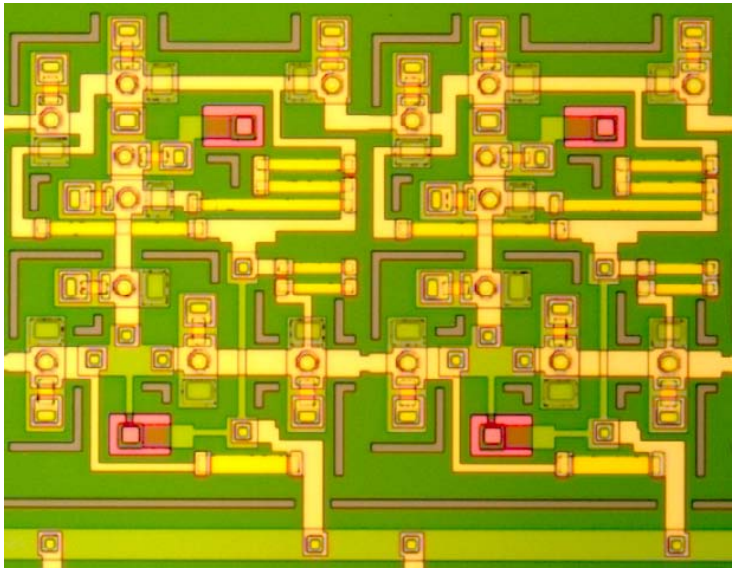






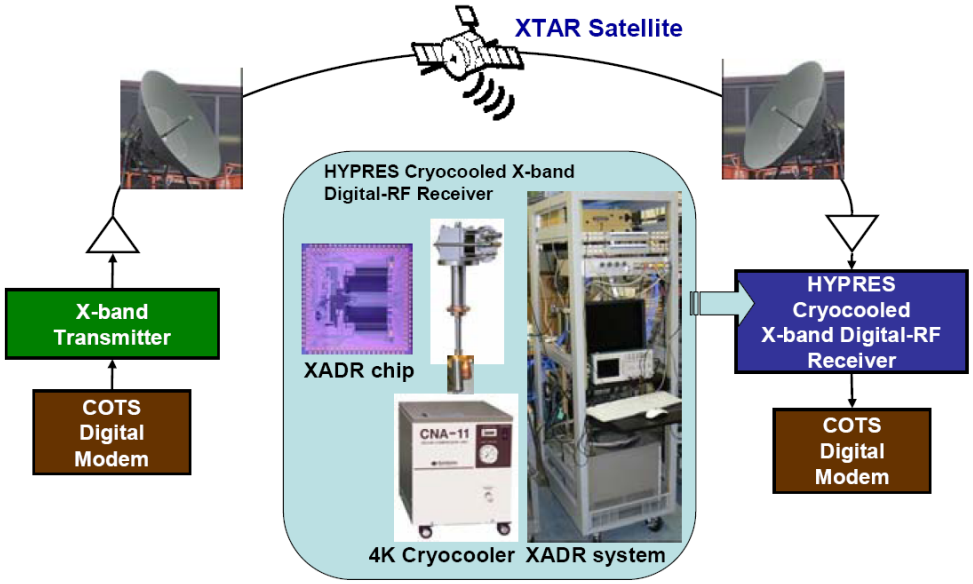
Fields of Application

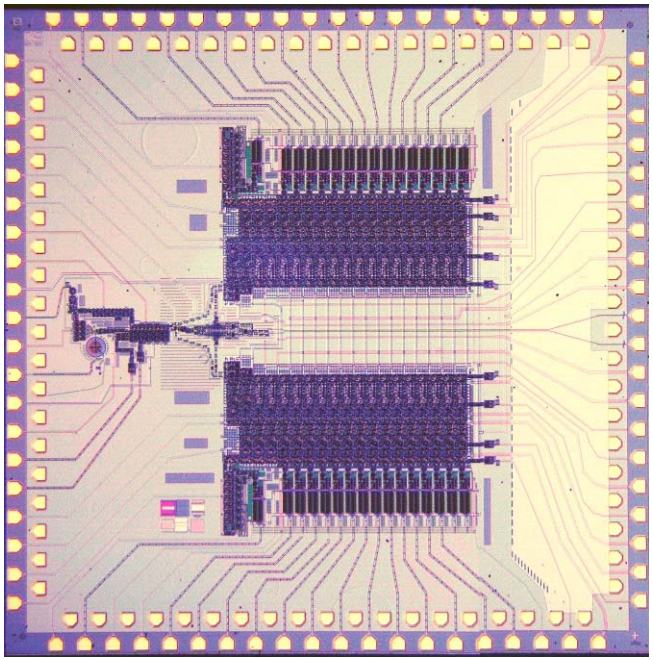
SFQ is not a technology for everyday devices but can do well at the high-end.

- High-speed computing.
- Telecommunication.
- Imaging.
- Mixed signal.

SFQ in Telecommunication

The All Digital Receiver (ADR) chips comprise either a low-pass or band-pass single loop delta modulator with phase modulation–demodulation architecture together with digital in-phase and quadrature mixer and digital decimation filters.



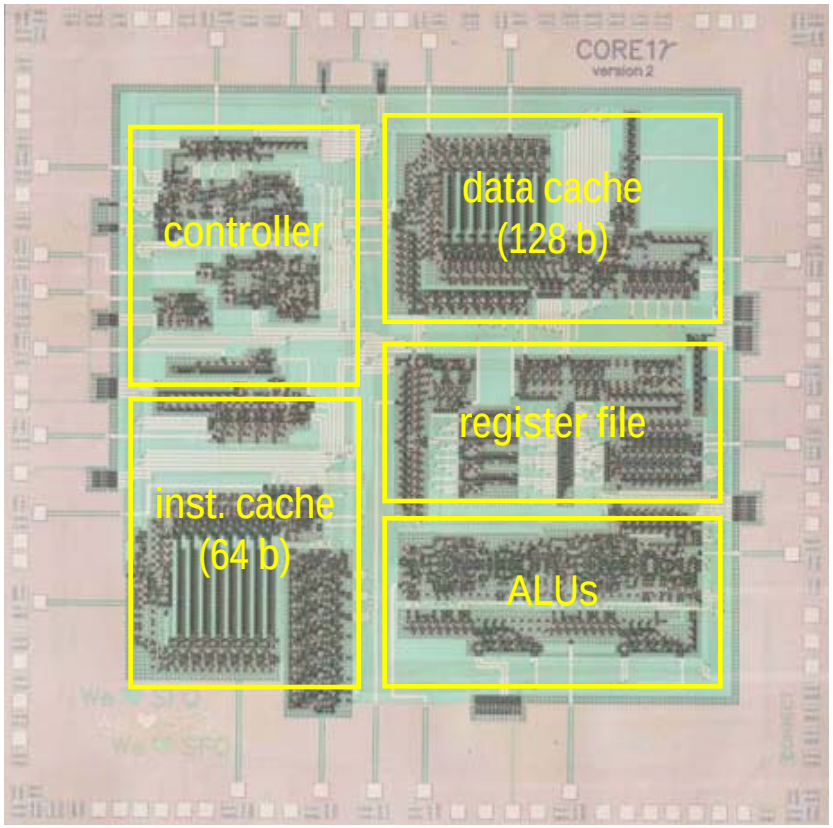


The Cryocooled X-band All-Digital Receiver (XADR) system demonstration with live XTAR satellite. Digital data including video were transmitted over satellite and received by HYPRES XADR system by directly digitizing X-band (7.6 GHz) satellite downlink signal with high sampling rate clock.

Microphotograph of the low-pass ADR 1 cm^2 chip (Hypres Inc.) containing 12,000 Josephson junctions clocked at 29.44 GHz. In the Nyquist band of 10 MHz, this chip shows 75.7 dB signal-to-noise-and-distortion ratio (SINAD).

SFQ Based Microprocessor

Most complex circuit realised in 10 kA/cm^2 process by ISTEC Japan.

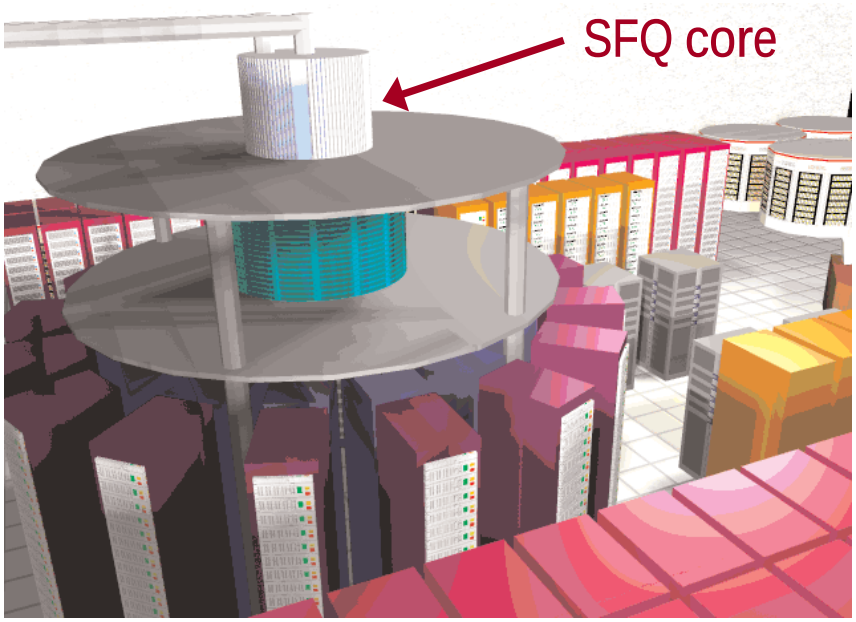


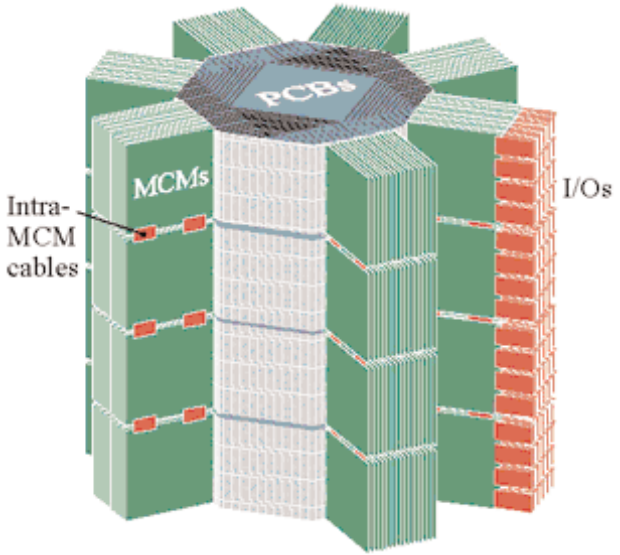
- 8 bit, bit-serial
- 1,000 MOPS at peak
- 25 GHz bit-operation
- 4-stage pipelining
- 22,302 JJs
- 2.63A (6.5 mW)
- 128-bit inst. Cache
- 64-data cache
- 6.3×6.3 mm^2
- 8 mm die

Photograph of the 8 bit serial microprocessor Core1γ (photo - courtesy of A. Fujimaki).

Background slide from N. Yoshikawa

Superconducting petaFLOP Computer





Design study of the system installation concept for petaflops computer. Enclosure for the superconducting processors is 1 m^3 white structure with cooling lines into the top (left hand side). Packaging concept showing 512 fully integrated multi-chip modules (right hand side).

NSA Study on Superconducting Technology Assessment, 2005

Conclusion

- Silicon has still a lot of potential: Performance instead of speed!
- SFQ is a technology for high-end devices.
- Works well on lab level, foundries are the next step.
- Comparatively simple thin-film technology: only metals and insulators.
- High performance can be reached already at moderate feature sizes: submicron range.
- Cooling needed but is not an issue.
- SFQ opens new performance levels in high-speed computing, telecommunication, ADC, mixed signal.

About SFQ

WHAT IS RSFQ CIRCUITRY?

Single Flux Quantum (SFQ) is the latest generation of superconductor circuits based on Josephson junction devices. It uses generation, storage, and transmission of identical single magnetic flux quantum pulses at rates approaching 1,000 GHz. Small asynchronous circuits have already been demonstrated at 770 GHz, and clocked SFQ circuits are expected to exceed 100 GHz.

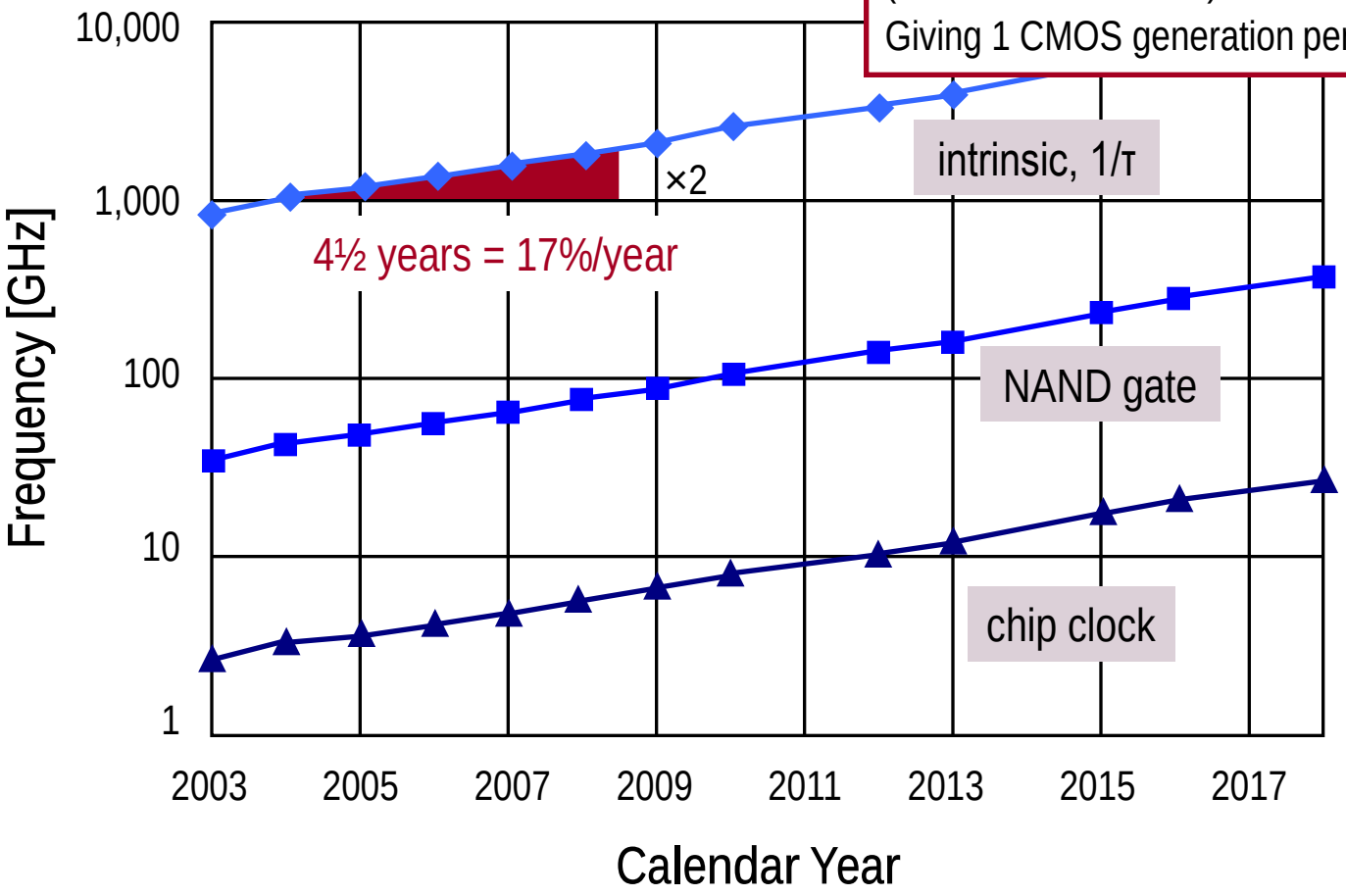
JOSEPHSON JUNCTIONS

The Josephson junction (JJ) is the basic switching device in superconductor electronics. Josephson junctions operate in two different modes: switching from zero voltage to the voltage state and generating single flux quanta.

The early work, exemplified by the IBM and the Japanese Josephson computer projects of the 1970's and 1980's, exclusively used logic circuits where the junctions switch between superconducting and voltage states and require AC power. SFQ junctions generate single flux quantum pulses and revert to their initial superconducting condition. RSFQ circuits are DC powered.

Moore's Law – Frequency Scaling

Historical grow rate = frequency ×2 every 4½ years
(meaning 17% per year, since $1.17^{4.5}=2$)
This corresponds to 2 CMOS generations
(since $F^{n+2}/F^{n}=1/k^{2}=2$)
Giving 1 CMOS generation per 2.25 years



Background slide from
P. Zeitzoff, Sematech