IBM Research – Zurich Laboratory

NEMS for ultra-low power logic applications

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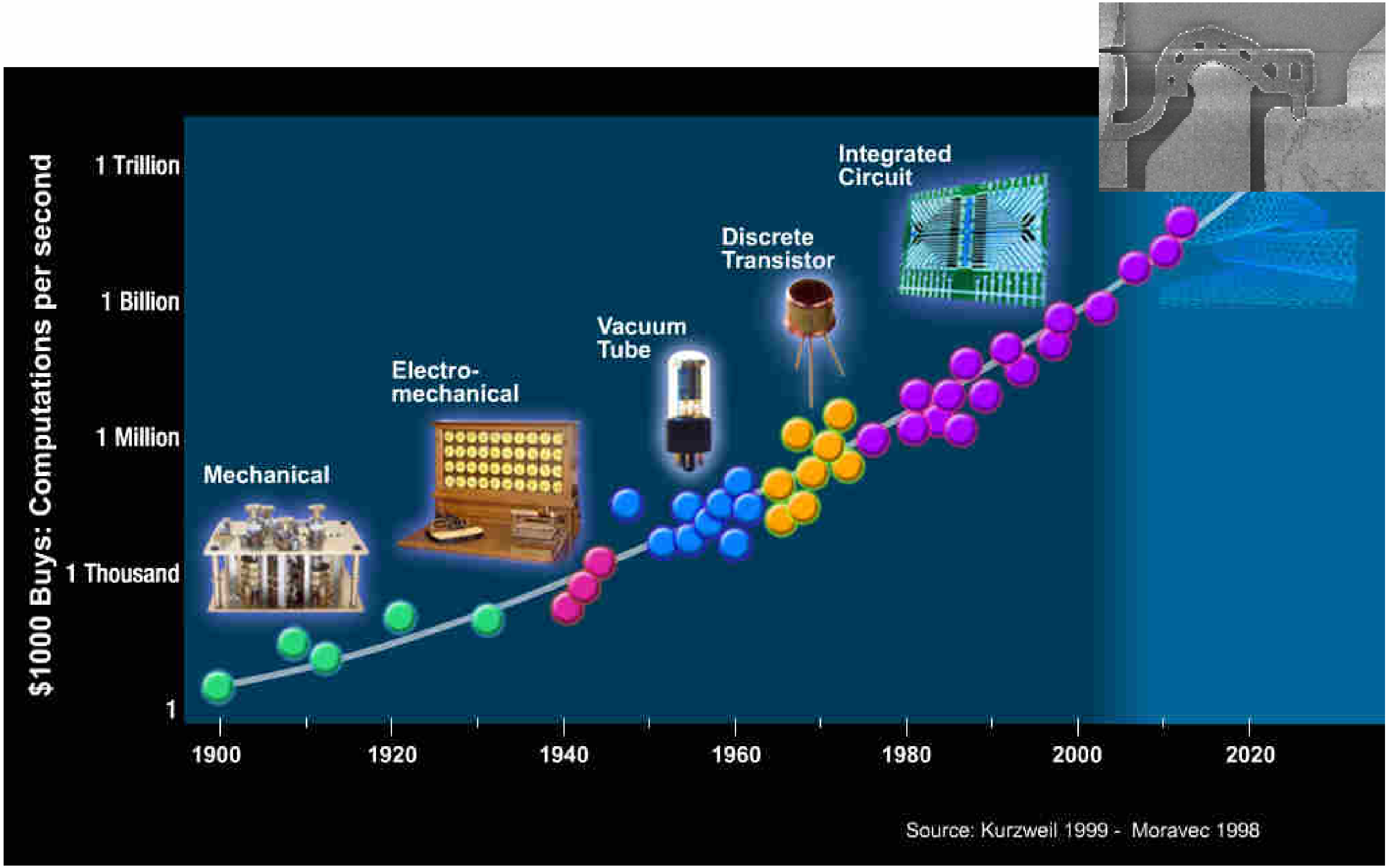
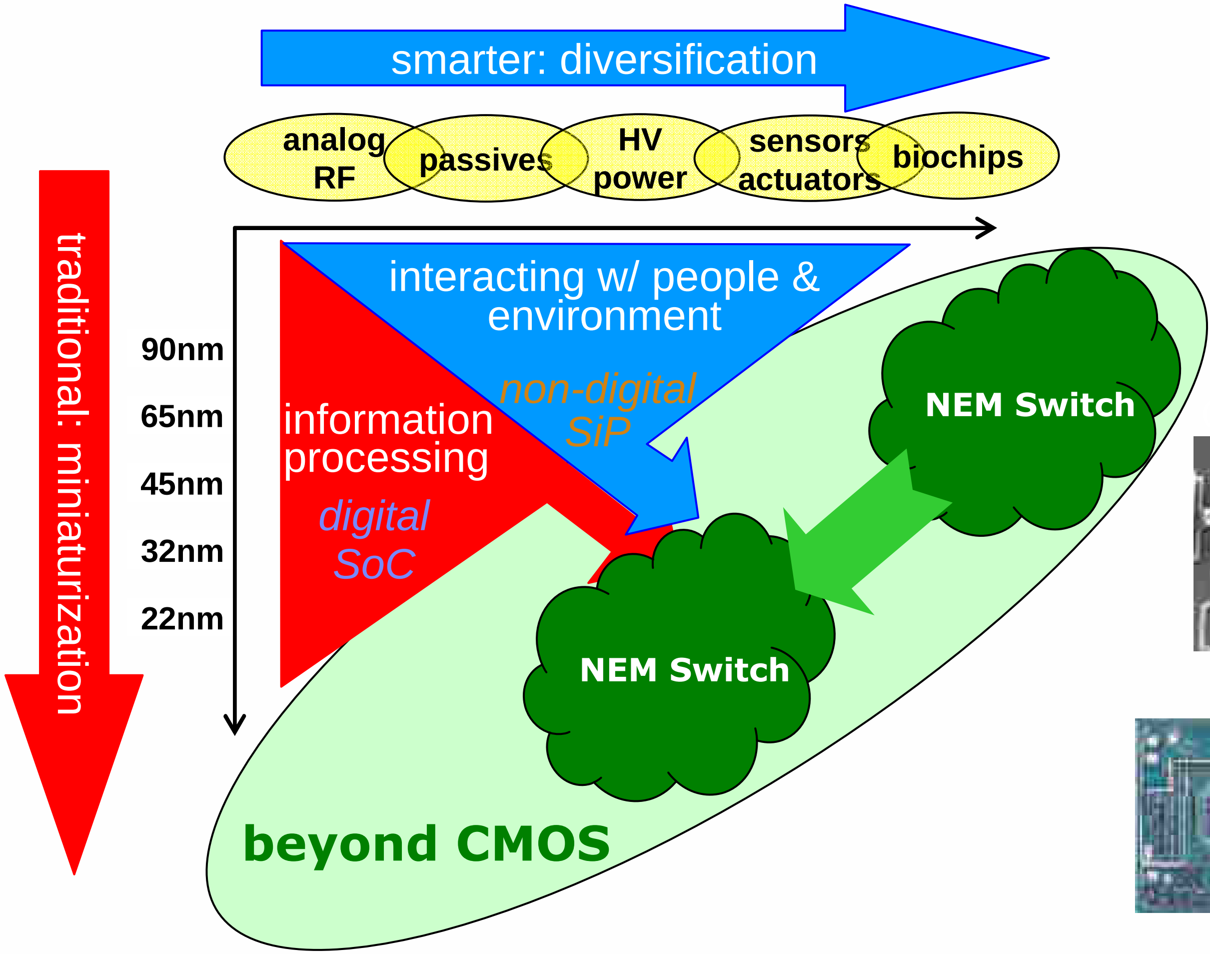
the evolution of information technology

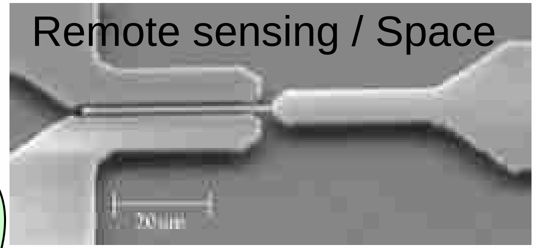


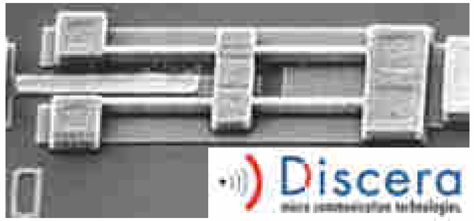
outline

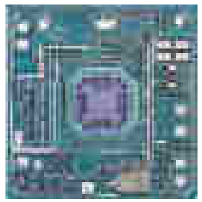
- **IT technology landscape**
- **NEM switch for logic applications**
- **NEM switch design and fabrication**
- **NEM switch circuits**

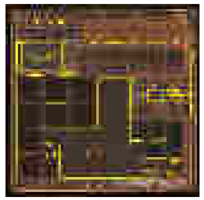
IT technology landscape: “more Moore” vs. “more than Moore”







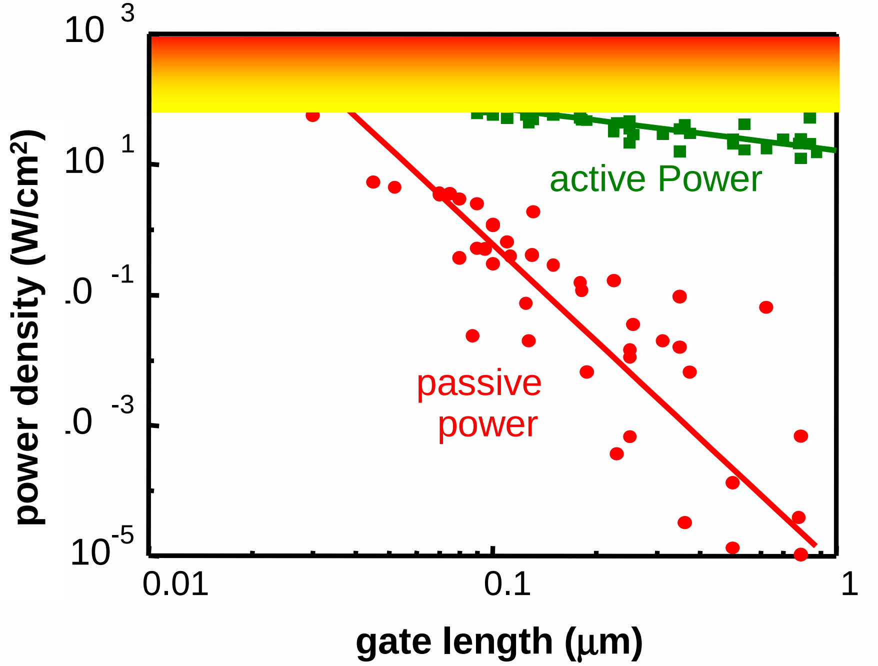




adapted from a graphic in the Executive Summary of the ITRS, 2007 edition

traditional miniaturization: CMOS challenges

- **power/energy challenge**
  - **power density critical**
  - **energy consumption too high for**
    - **autonomous devices**
    - **exascale computing**
  - **leakage power approaches active power**
- **functionality challenge**
  - **sensors and actuators**
  - **filters**
  - **other analog functionality**
  - **dormant devices (mostly Idle)**
  - **devices in harsh environments**
    - **high temperature**
    - **radiation-hard**



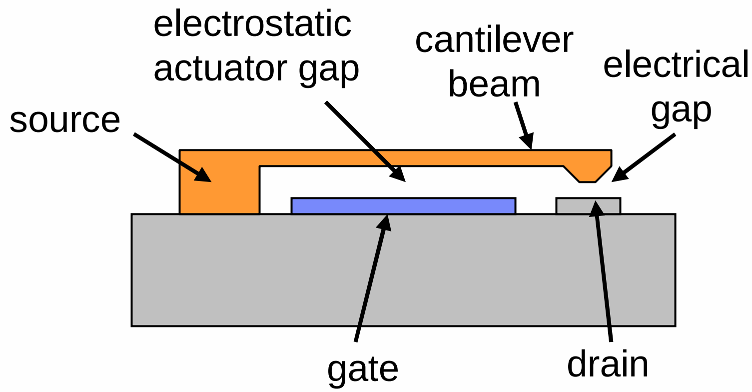
traditional miniaturization: NEM switch opportunities

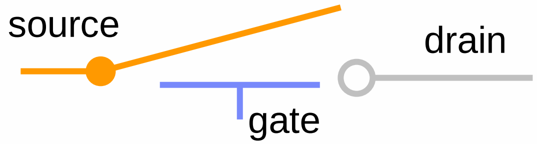
power / energy efficiency
- zero leakage
- high on-current
- virtually infinite sub-threshold slope

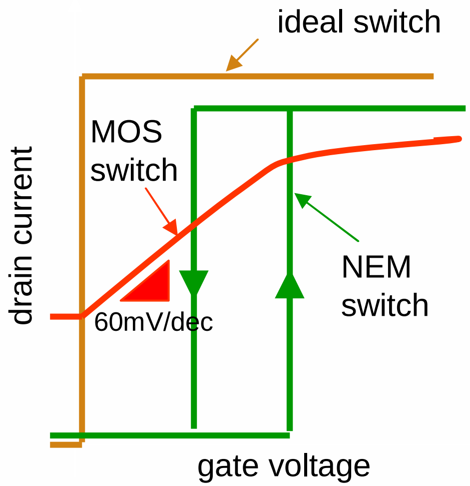
harsh environments
- inherently radiation-hard
- high temperature devices shown

functionality challenge
- logic
- memory
- filters
- sensors
- actuators

cost pressure
- less lithography steps
- no implant







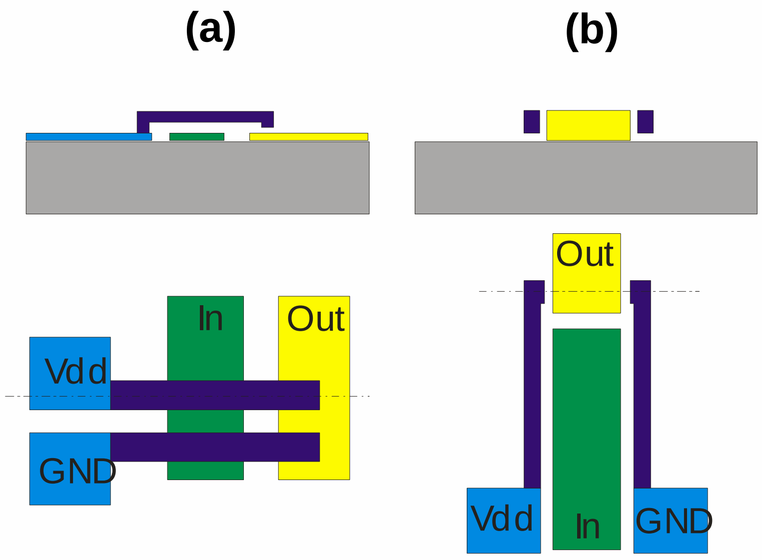
NEM switch design

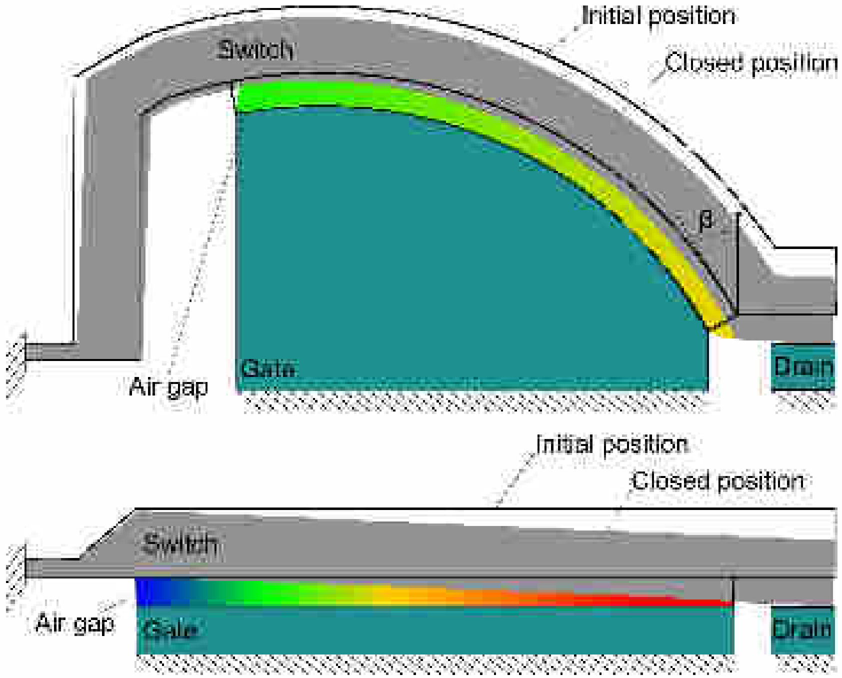
in-plane (b) vs. out-of-plane (a) offers

- **freedom of design**
- **symmetric layers**
- **scalability**

curved vs. straight design offers

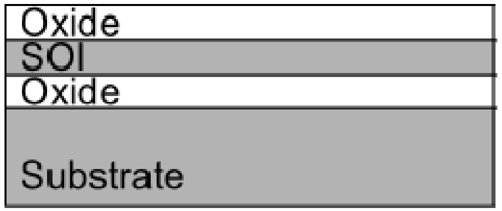
- **robustness through control of the electric field**
- **scalability through single, sublithographic actuation gap for actuation and electric contact**





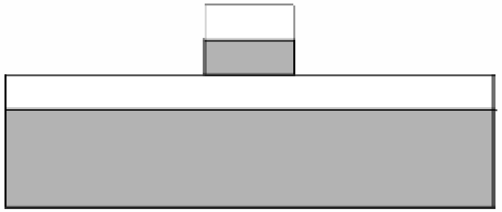
NEM switch fabrication

SOI w/ thermal oxide



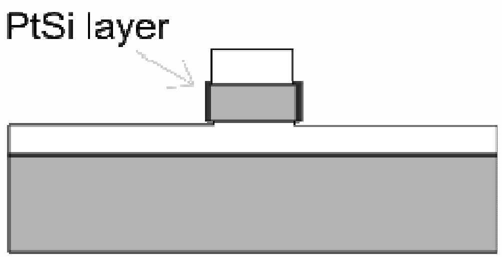
a)

RIE (moving part)



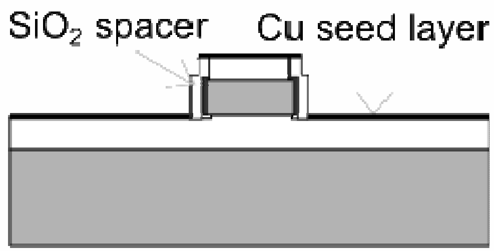
b)

silicidation



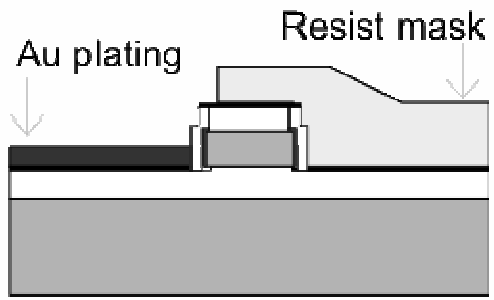
c)

sacrificial layer & seed layer deposition



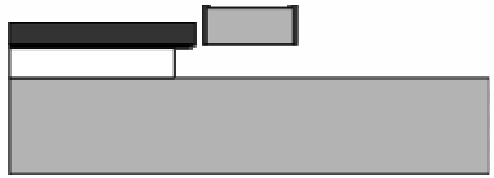
d)

Au electroplating



e)

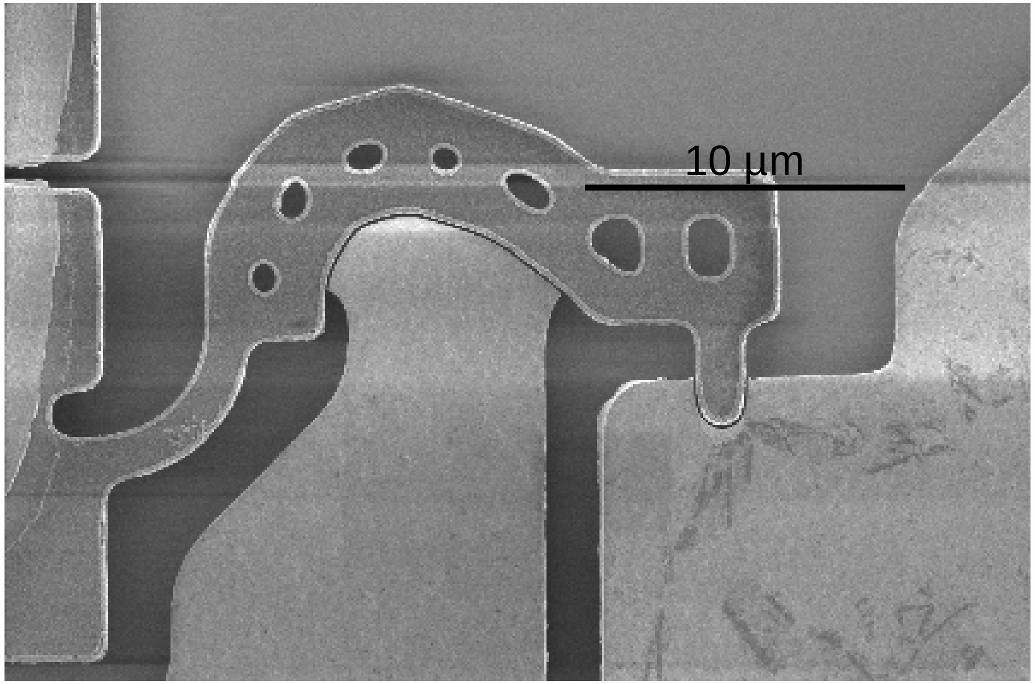
release

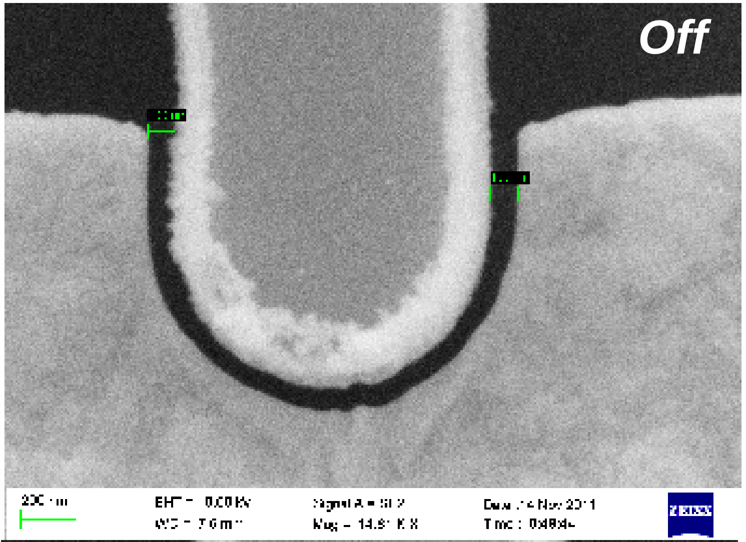


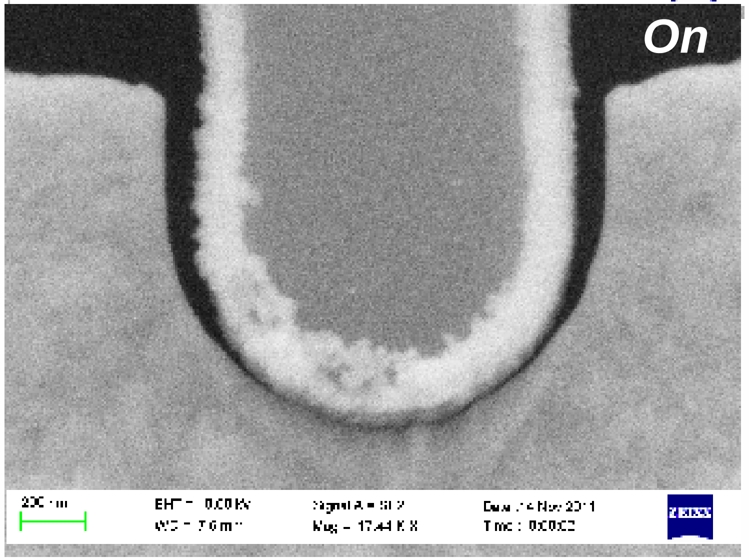
f)

D. Grogg, EIPBN 2012

NEM switch fabrication

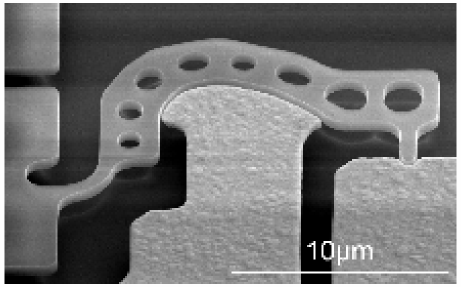


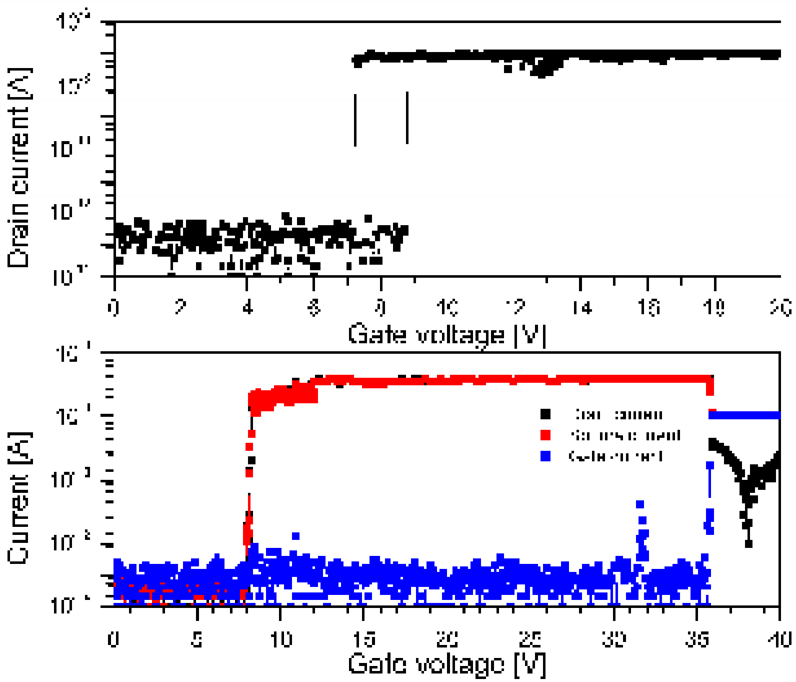


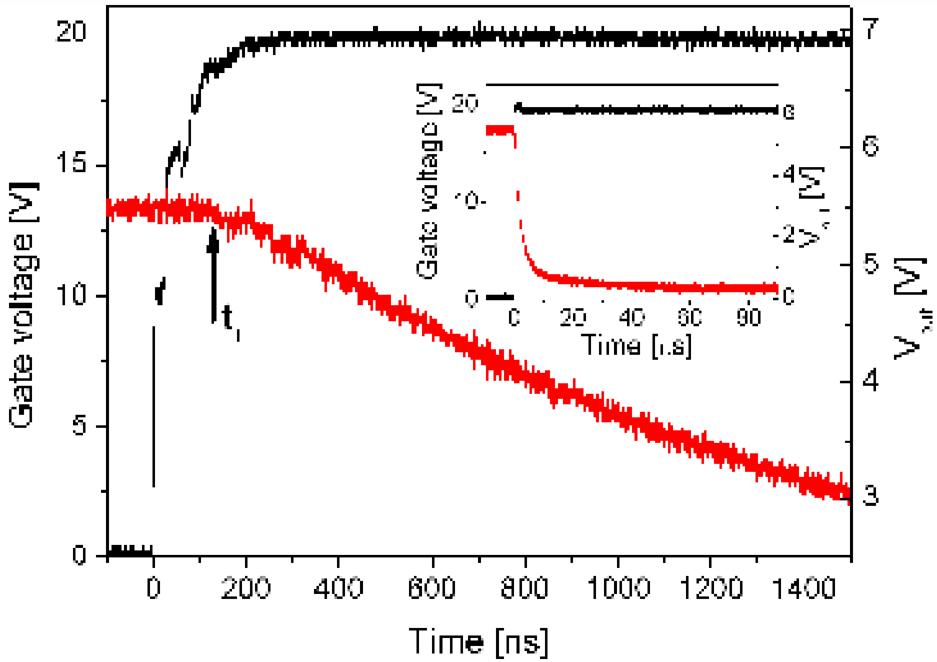


NEM switch characterization

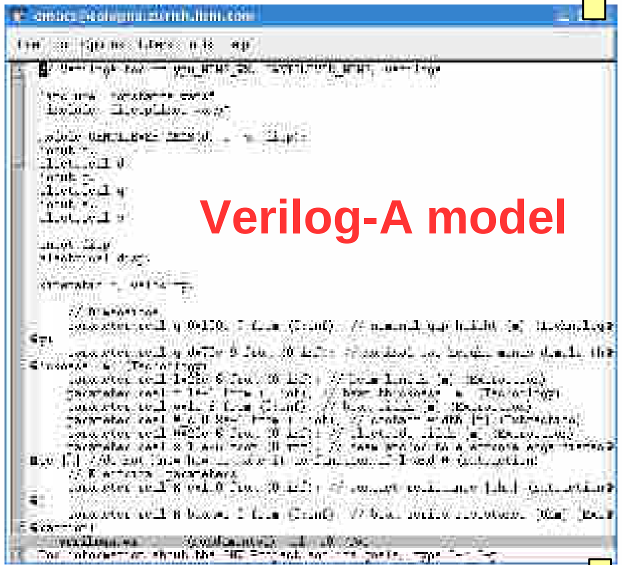
- **actuation voltage matches results predicted by simulation**
- **switch breakdown at >3x overdrive**
- **electrical contact @ 130ns**



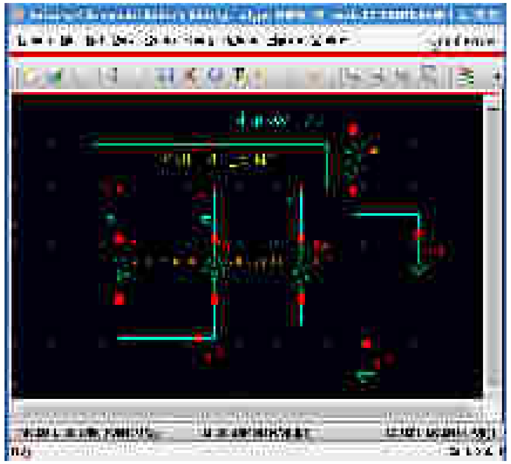




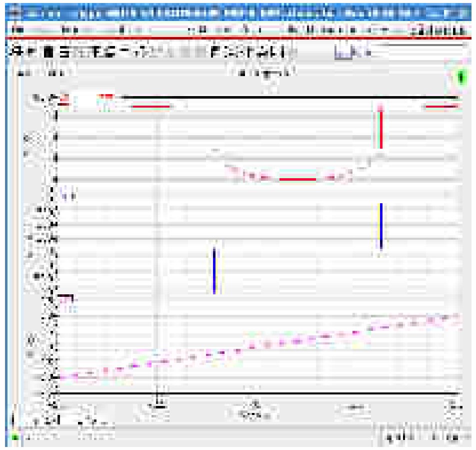
NEM switch circuit design / modeling



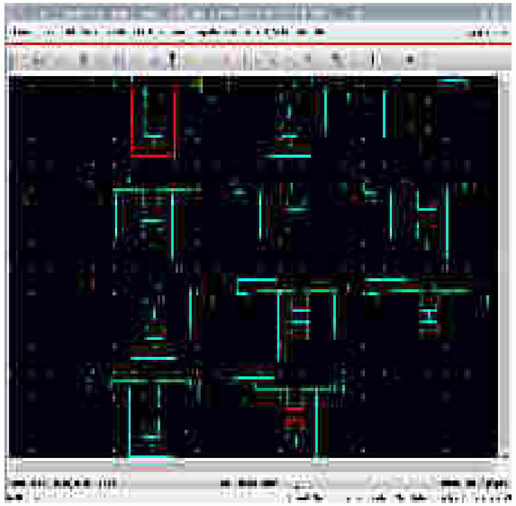
I. device modeling



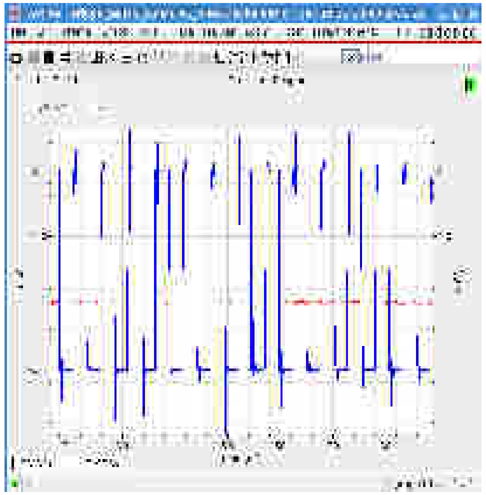
II. single device



III. device simulation

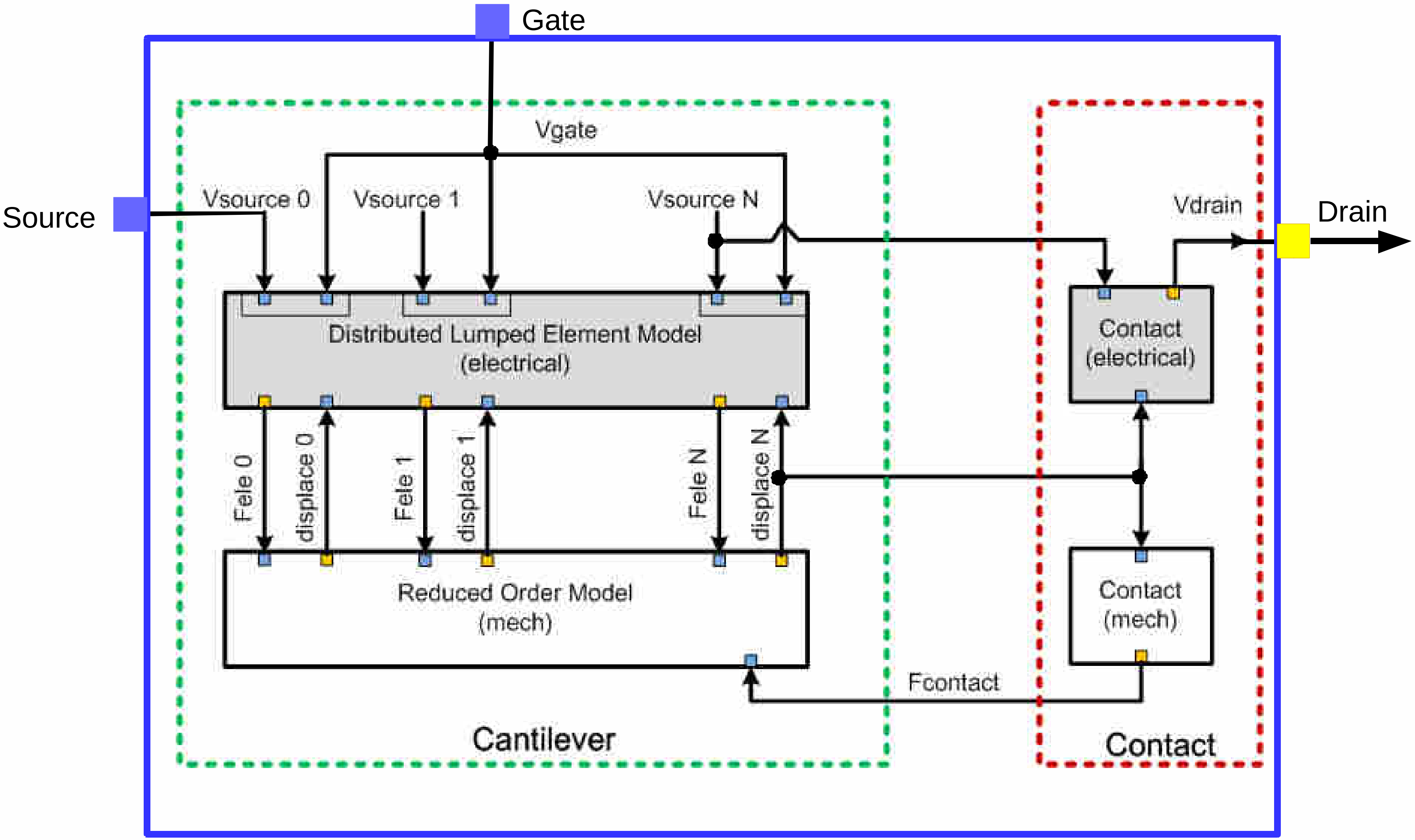


IV. composing circuit

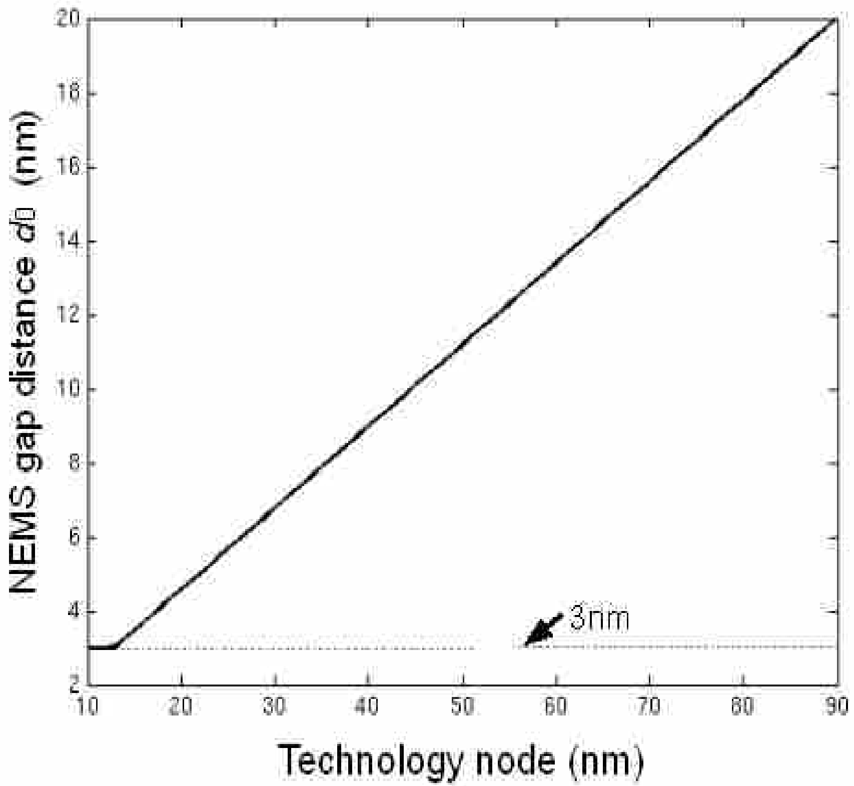


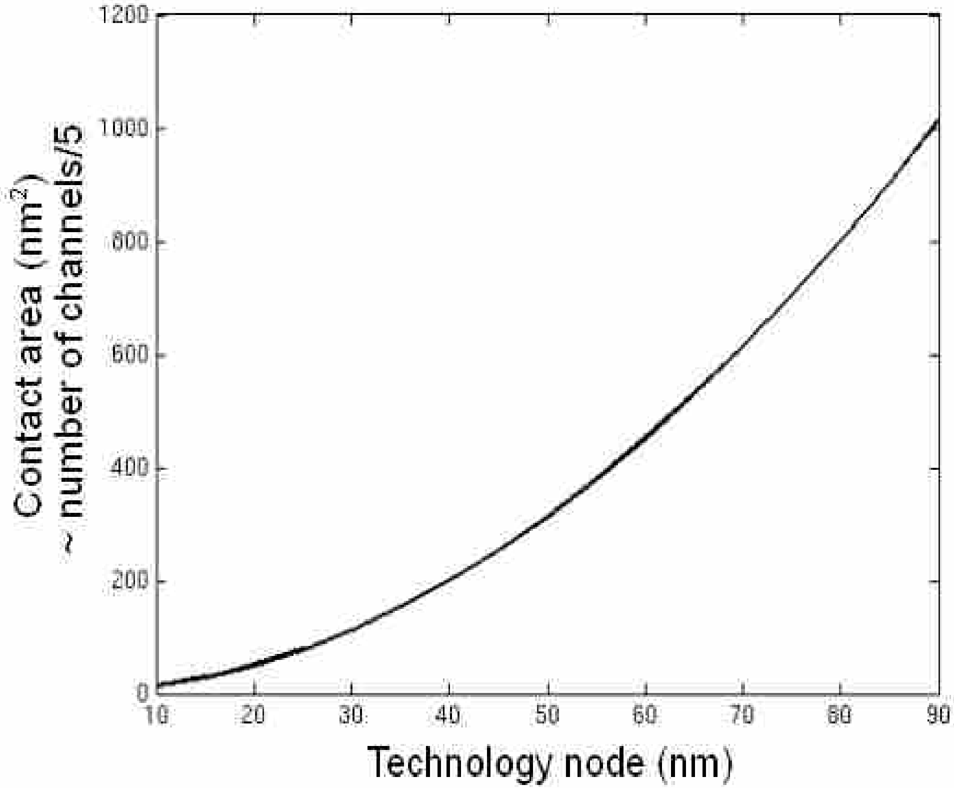
V. circuit simulation

NEM switch model



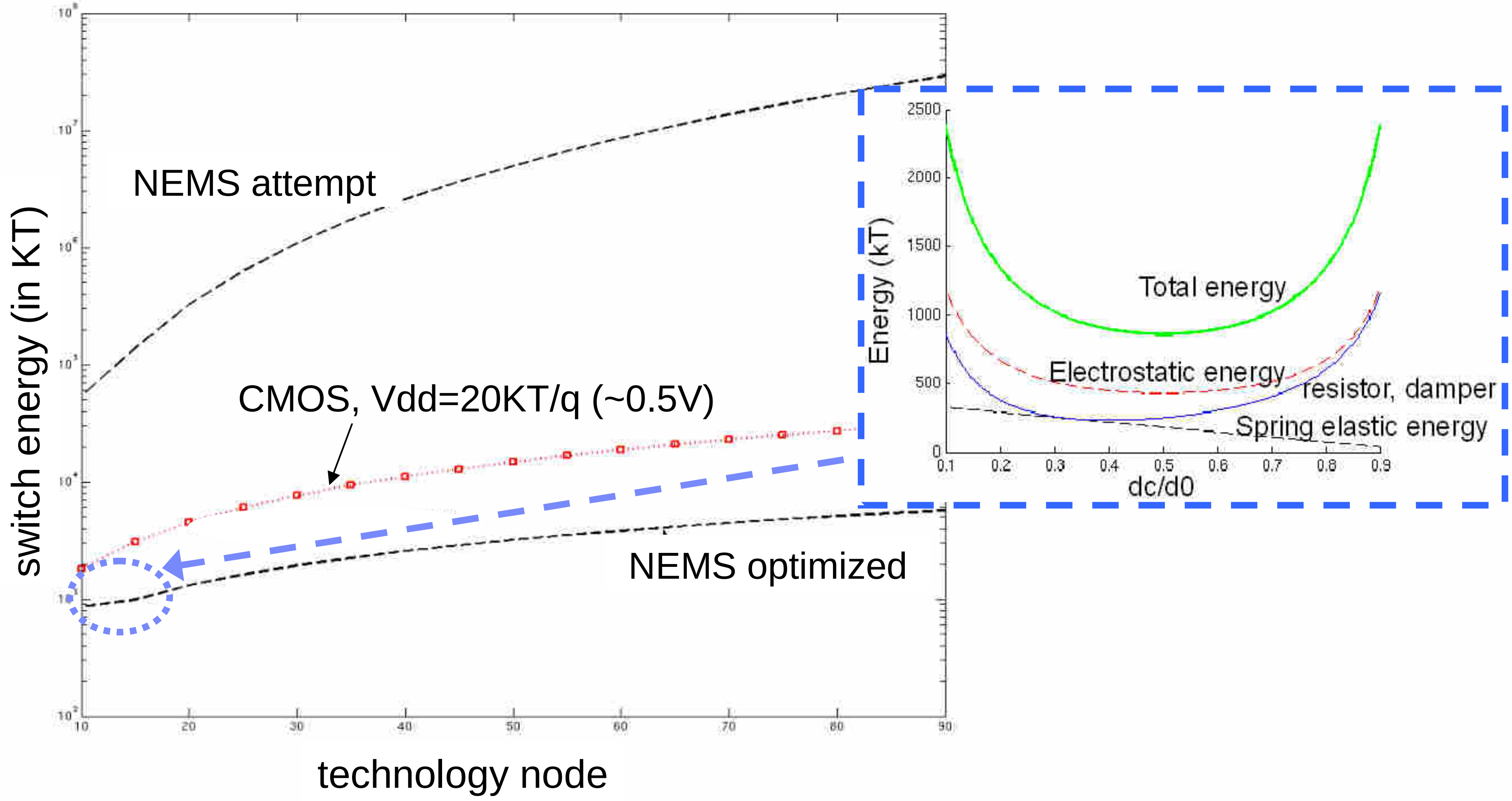
NEM switch scaling



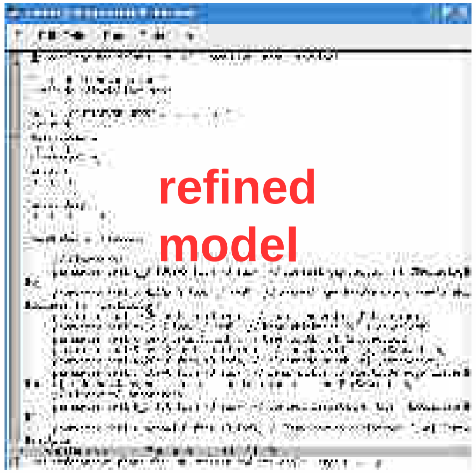


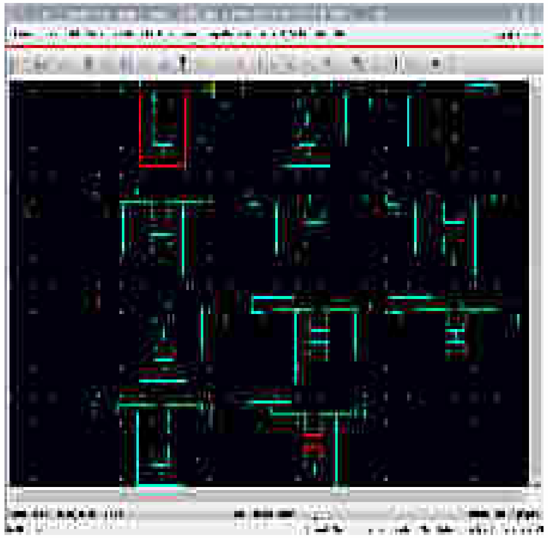
- **predicted minimum gap distance 3nm**
- **predicted contact area = *N*²/8; (*N* is technology feature size)**
- **No. of channels = 5*contact area; (assuming 5 channels/nm²)**

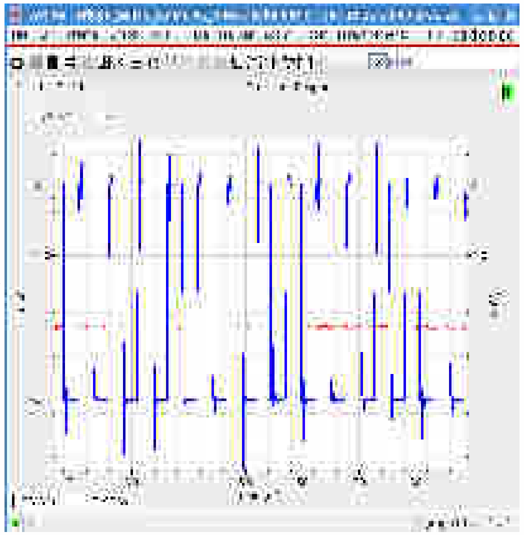
NEM switch energy @ device level



NEM switch circuit simulation

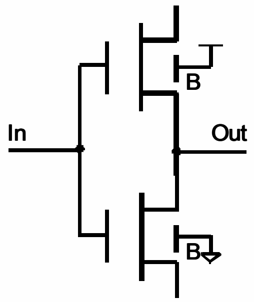




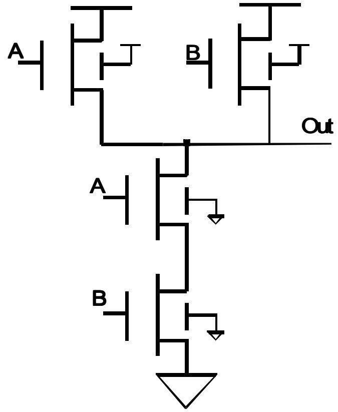


NEM switch logic styles: area optimization

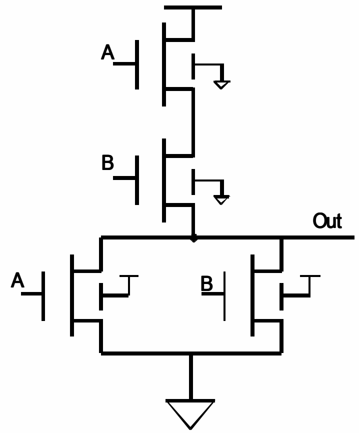
1. Static logic, examples:



(a) INV

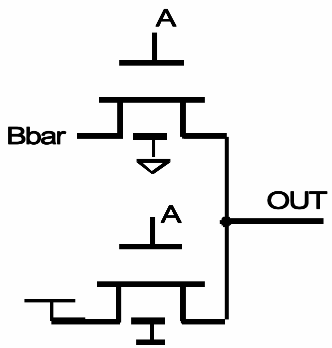


(b) 2-input NAND

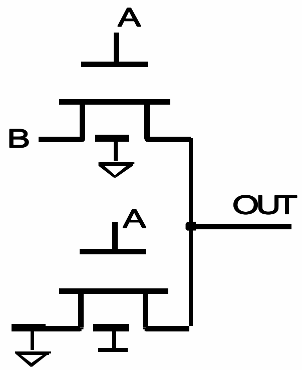


(c) 2-input NOR

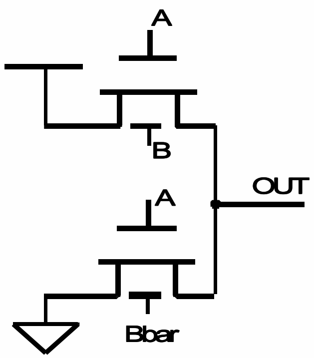
2. Transmission gate logic, examples:



(d) 2-input NAND

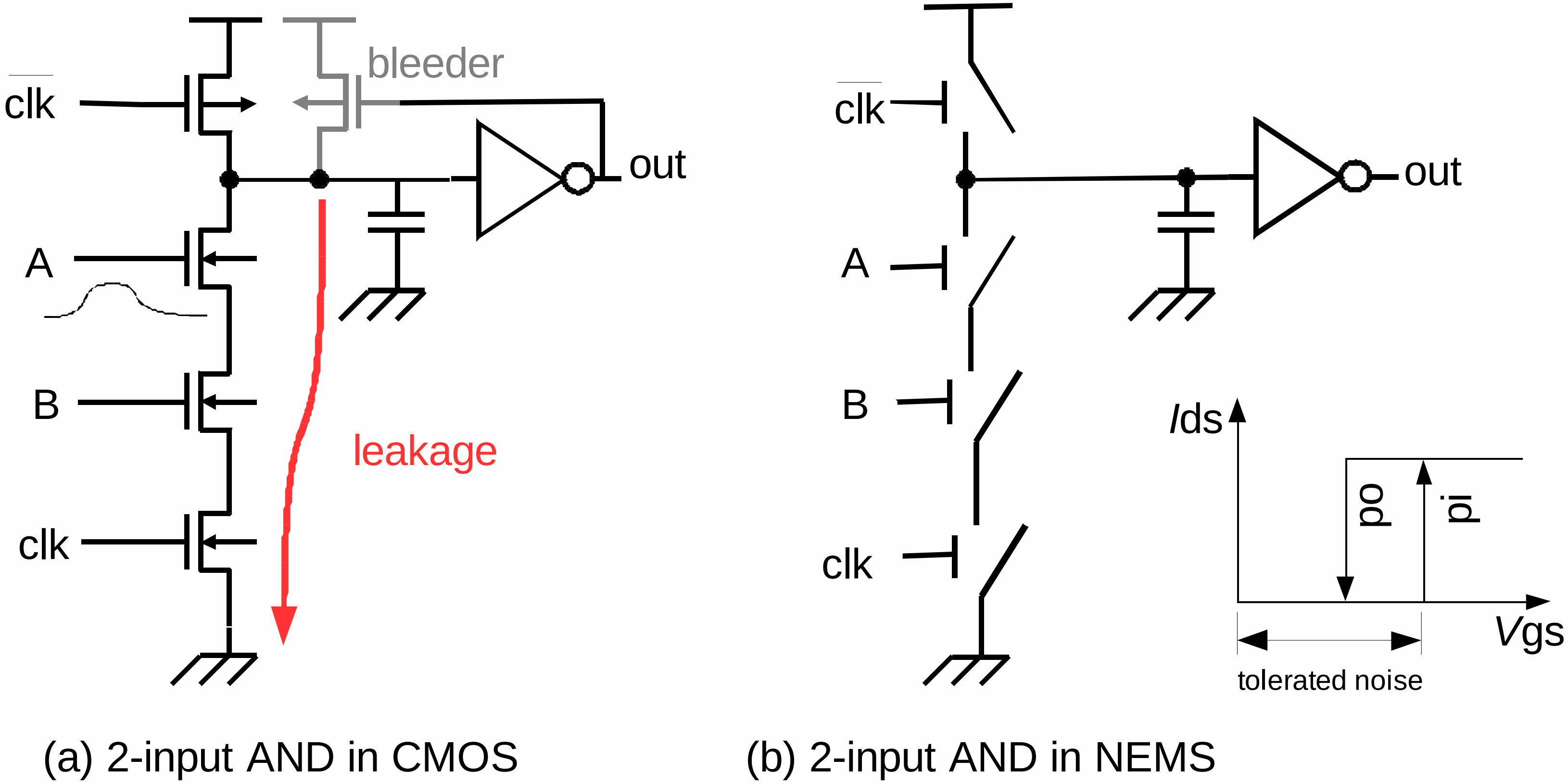


(e) 2-input AND



(f) 2-input XOR

NEM switch dynamic logic: energy optimization



- **noise on input ports does** NOT **cause pre-charging**
- **bleeder is** NOT **needed, as NEMS has zero leakage**

summary

- **NEM switch opportunities**
  - **energy efficient computing**
  - **autonomous devices**
  - **sensors / actuators**
- **NEM switch challenges**
  - **scaling**
  - **contact reliability**
- **NEM switch circuits**
  - **virtually zero stand-by power**
  - **potentially outperforms CMOS in terms of energy efficiency**
  - **new logic styles and architectures**

next steps

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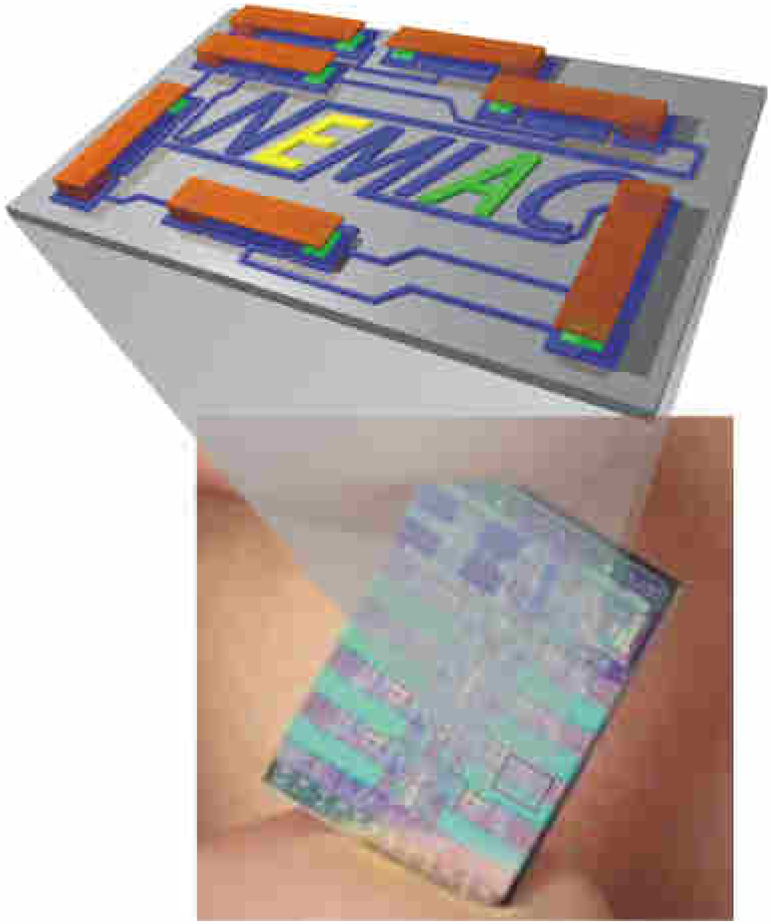

Thank you