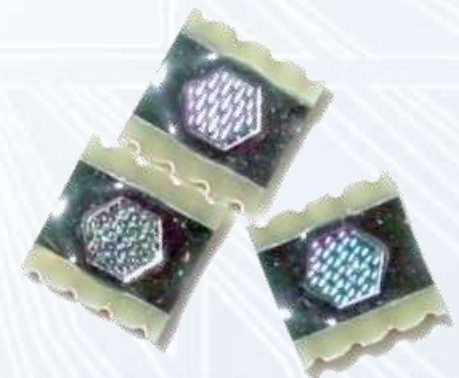
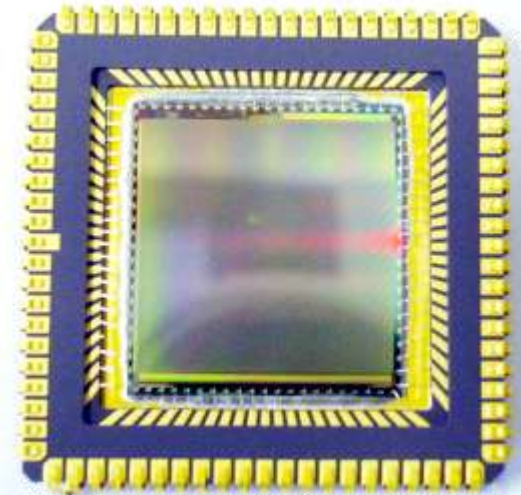
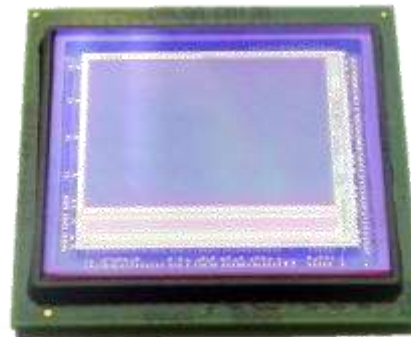
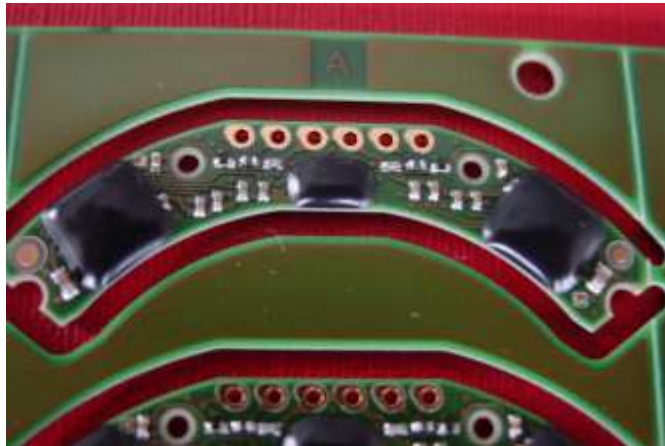


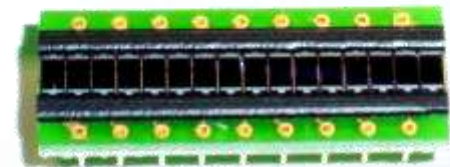
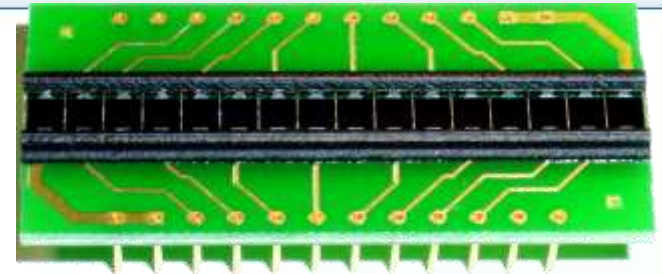
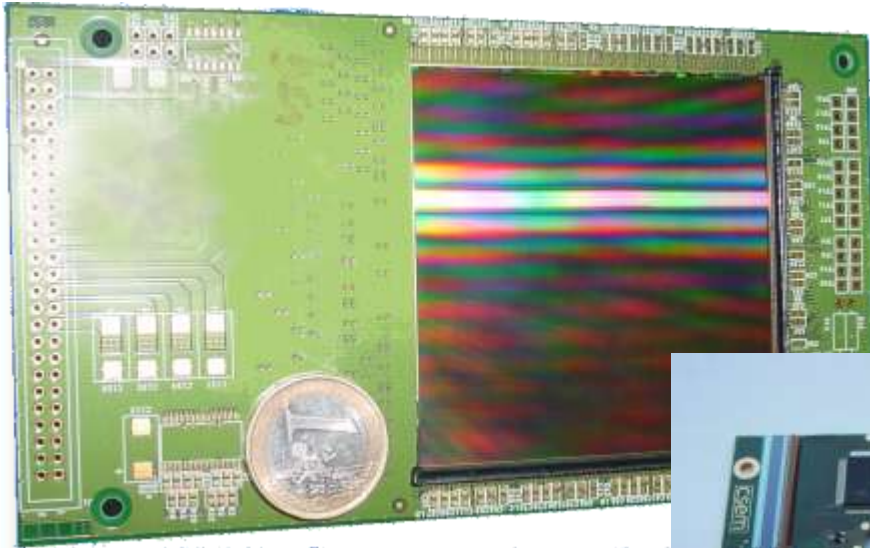


Aufbau- und Verbindungstechnik für optische Sensoren in der Medizintechnik

Gregor Woldt / Werner Schneider
MPD GmbH Dresden

Sensorbeispiele im Microelectronic Packaging



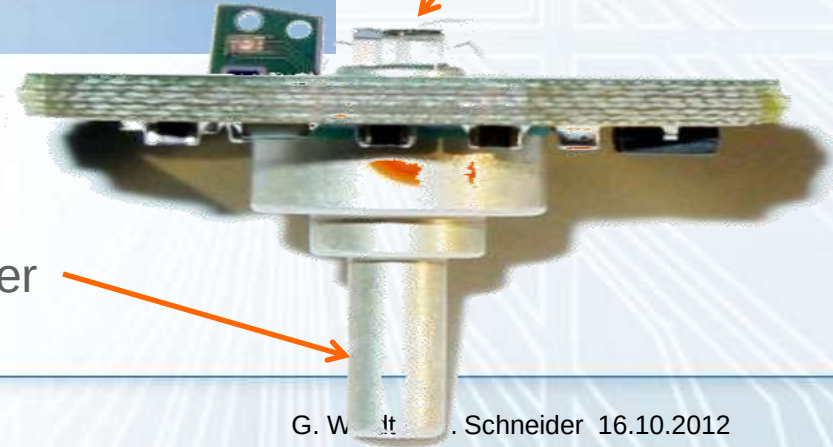
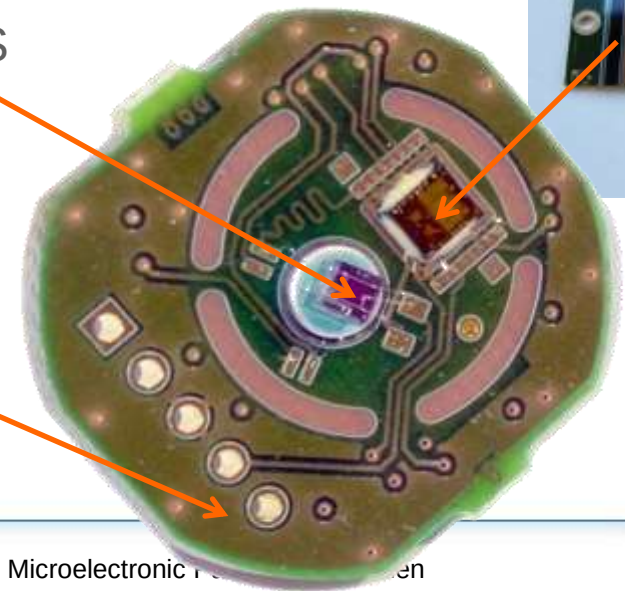


MEMS

MEMS

PCB

Carrier

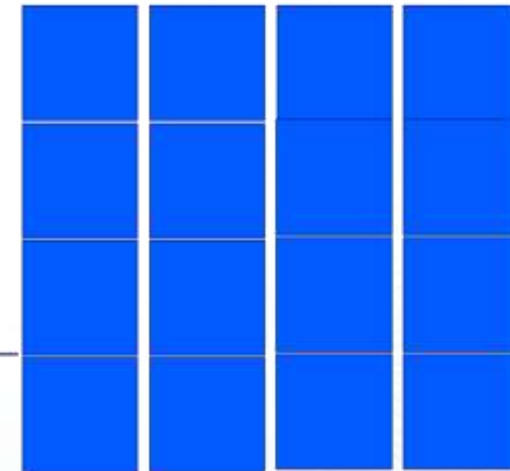
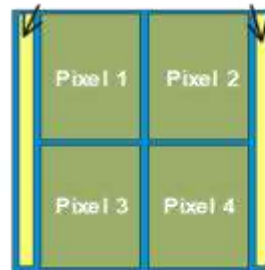


■ Anfrage

Packagingtechnologie für ein opto-elektr. Sensor array → **digital Silicon Photomultiplier dSiPM**

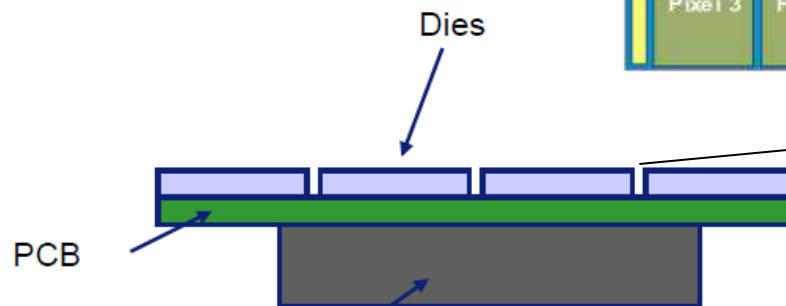
Array, 4 x 4 dies

Die, ~ 8 x 8 mm²



these gaps should be as small as possible

Glasabdeckung + Szintillator



Connector on back side of PCB

- Technisch / technologische Herausforderung

PCB – Entwicklung (Layout, Technologiekonzept)

Die – Bonden

Wire – Bonden

Glas – Montage

Weiterverarbeitungsanforderungen beim Kunden

Packaginggesamtkonzept (Layout, Werkstoff, Technologie)

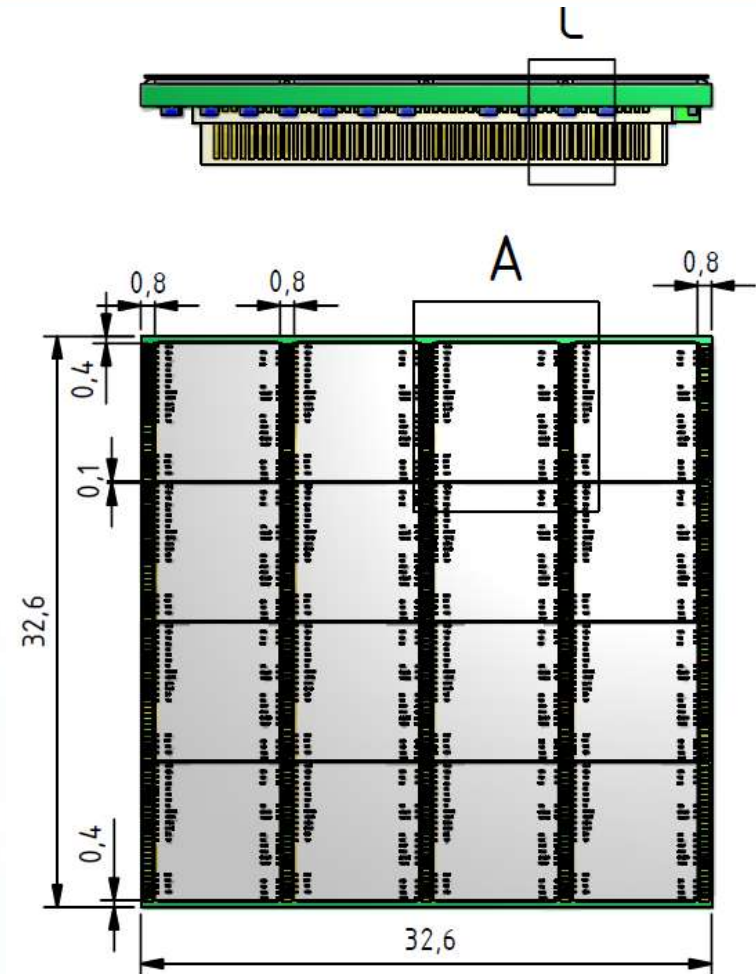
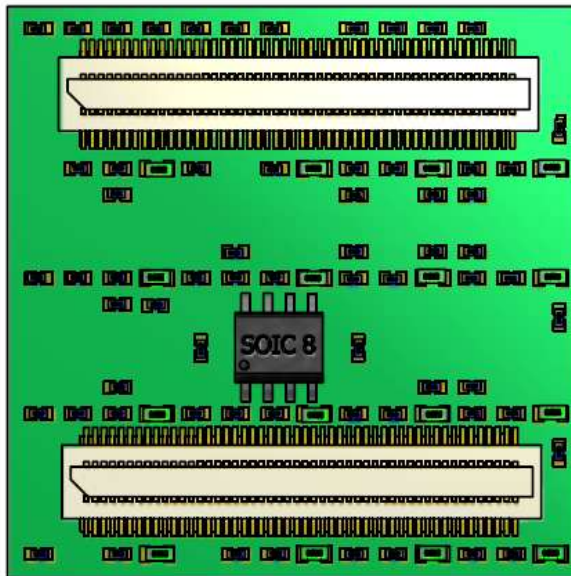
Zuverlässigkeitsanforderungen (-20°C/+75°C)

→ Anforderungen gehen weit über die der bisherigen Standardmodule wie Imagesensoren, Photodiodenzeilen, Power LED`s etc, hinaus

■ Aufgabenstellung / Spezifikation

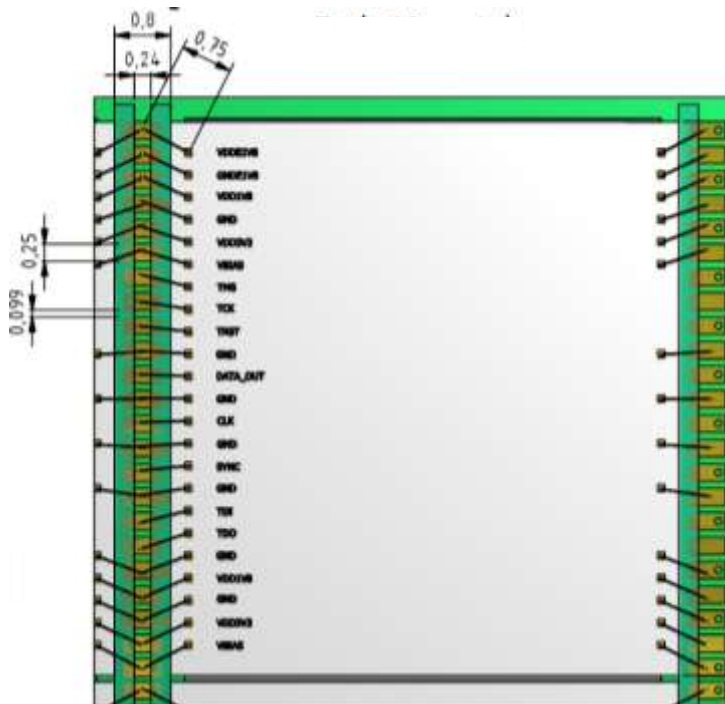
- PCB: 32,6 x 32,6 mm²
- Abstand Die zu PCB ohne Drahtbonds: 0,4 mm
- Abstand Die zu PCB mit Drahtbonds: 0,8 mm
- Abstand Die zu Die ohne Drahtbonds: 100 µm
- Abstand Die zu Die mit Drahtbonds: 800 µm
- Abdeckung Chip-Array mit Glas: 0,2...0,1 mm
- Abstand Glas zu Chipoberfläche: <100 µm
- PCB Krümmung: <100 µm
- Die-Krümmung <10 µm (Die-Biegeradius > 1m)

■ Lösungskonzept

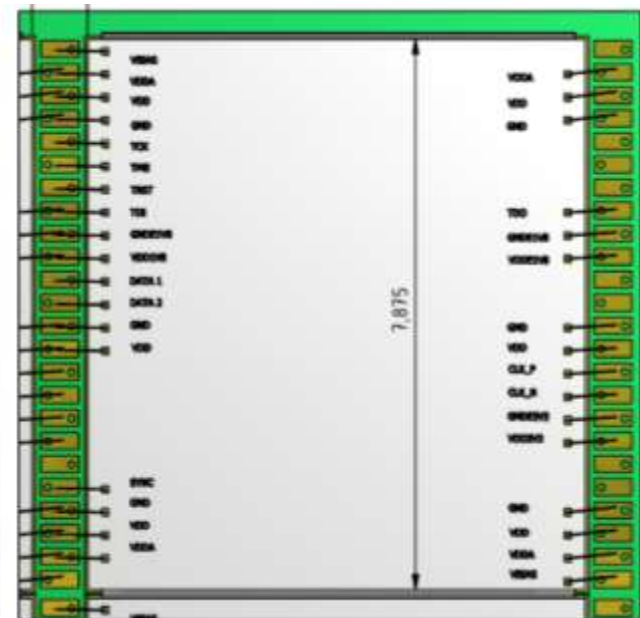


Neu: FBGA, Zunahme der SMD - Komponenten

■ Chip- und Bondbereich



Erstes Kundenchiplayout



"Packaginggerechtes Layout"

- Layoutentwicklung
 - COB nur Top Side
 - Drahtbondpadbreite $> 100 \mu\text{m}$
 - SMD nur Bottom Side
 - SMD-Platzierung $\Rightarrow$ symmetrisch
 - Randbereich frei von SMD`s
 - Stecker mittig
 - IC mittig
 - Verdrahtung fertigungsgerecht
 - Lagenaufbau $\Rightarrow$ symmetrisch (6, 10 $\Rightarrow$ 8)
 - Marken für SMD und COB
 - Nutzengestaltung
 - Automatengerechte Fertigung in mittleren Stückzahlen

■ Platinenaufbau

Stackup

Layer	Min	Max	Nom.	Tol-	Tol+	Thickness (Millimeter)	Stackup Picture	Family	Description	Type
smfr						0,0200		Prob 65 (Hal.Free)	Prob 65 Green	
epfr	0,0250	0,0400	0,0250		0,0150	0,0350		Cu	12μ + 25μm	SIGNAL - Foil
						0,0089		R1551W	1080 (0073)	
ip2	0,0150	0,0350	0,0150		0,0200	0,0230		Cu	18μ_d8 z12 + 13μm	SIGNAL - Foil
						0,0461		R1551W	0106 (0058)	
ip3	0,0150	0,0350	0,0150		0,0200	0,0270		Cu	18μ_d8 z5-B + 20μm	SIGNAL
						0,3000		R1566W	0300	
ip4					0,0990	0,0150		Cu	18μ	SIGNAL
						0,1985		R1551W	7628 (0204)	
ip5					0,0990	0,0150		Cu	18μ	SIGNAL
						0,3000		R1566W	0300	
ip6	0,0150	0,0350	0,0150		0,0200	0,0270		Cu	18μ_d8 z5-B + 20μm	SIGNAL
						0,0498		R1551W	0106 (0058)	
ip7	0,0150	0,0350	0,0150		0,0200	0,0230		Cu	18μ_d8 z12 + 13μm	SIGNAL - Foil
						0,0689		R1551W	1080 (0073)	
epba	0,0250	0,0400	0,0250		0,0150	0,0350		Cu	12μ + 25μm	SIGNAL - Foil
smba						0,0200		Prob 65 (Hal.Free)	Prob 65 Green	
						0,1650	Total Thickness (Calculated)			
						0,1000	Incl.Mask over Laminate (Customer)			
						0,1240	After Press (Customer)			
							+0,1200	-0,1200		
							+0,1180	-0,1180		

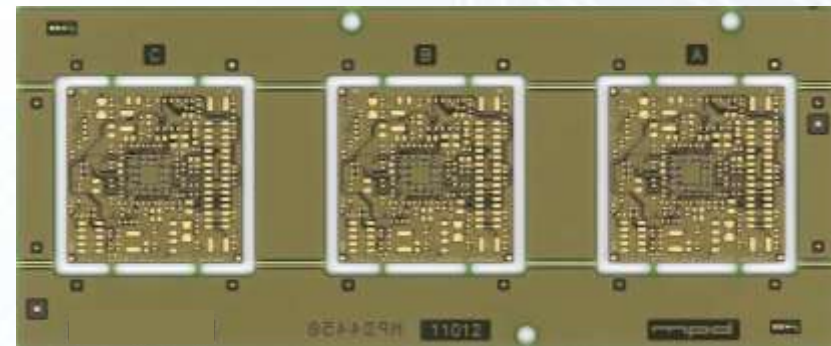
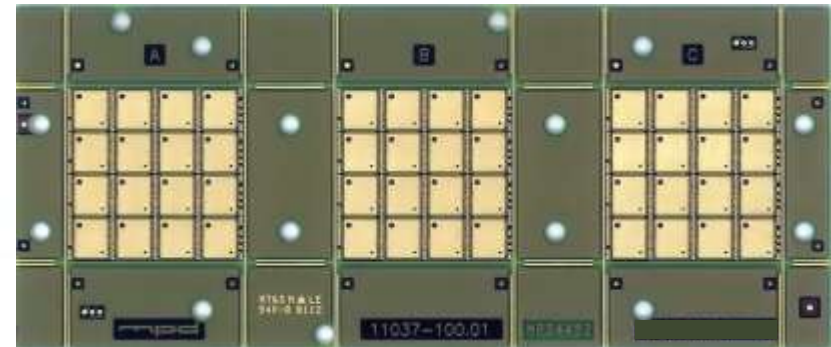
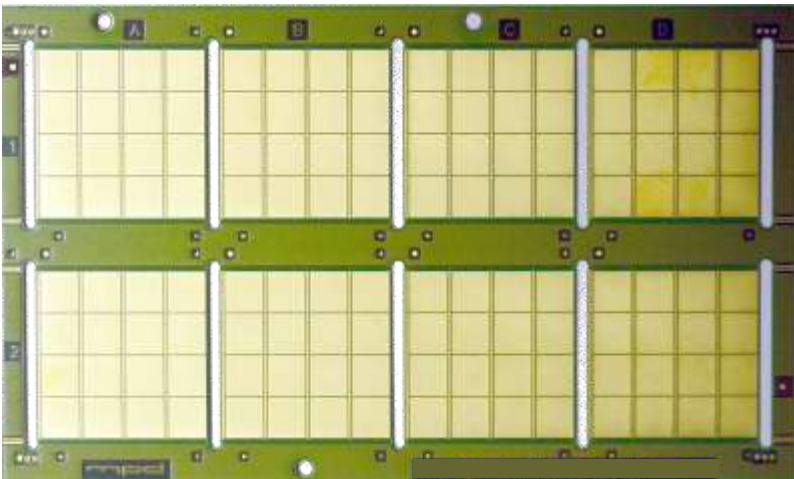
Microvias L1 → L2, L3; L8 → L7, L6

Prinzipieller Lagenaufbau: Kombination Plugging + MicroVia

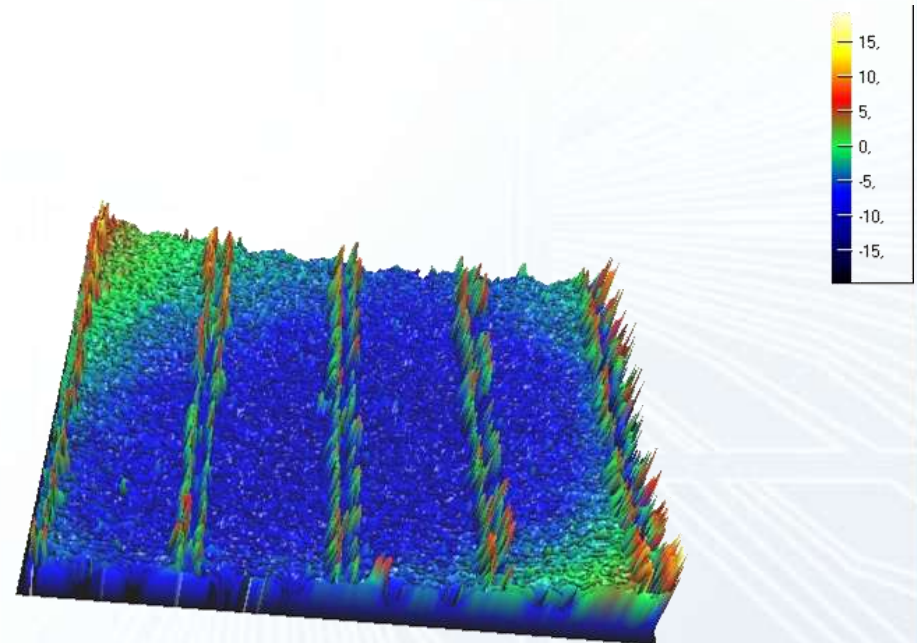
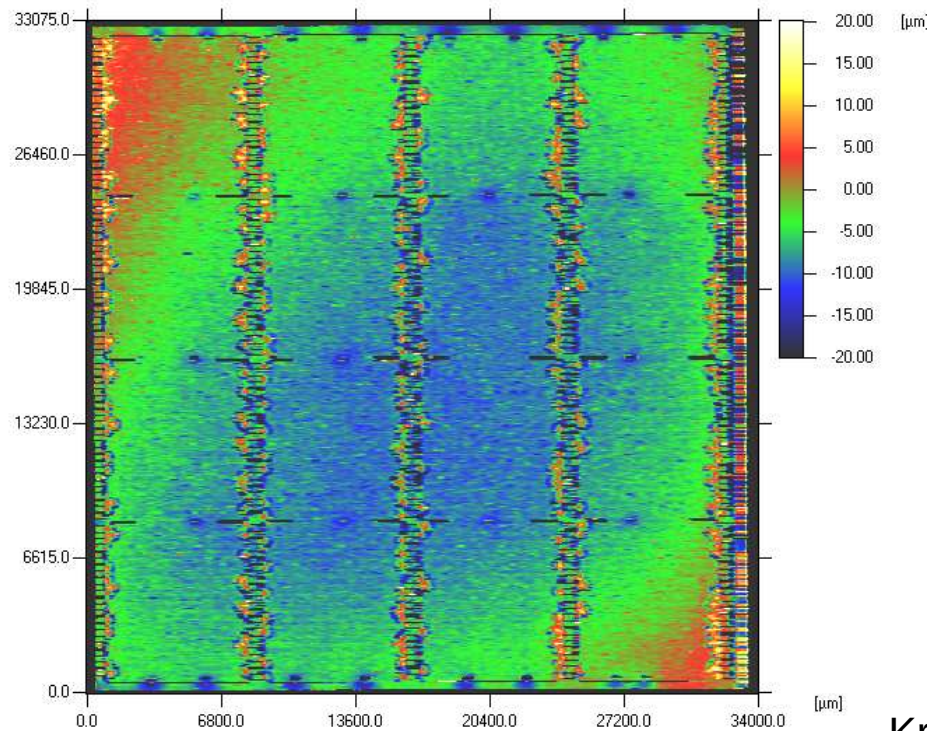
2 – 4 – 2 Aufbau



- Nutzengestaltung
 - Marken für SMT und COB
 - Sägenmarken
 - Justierhilfen
 - Produktkennung

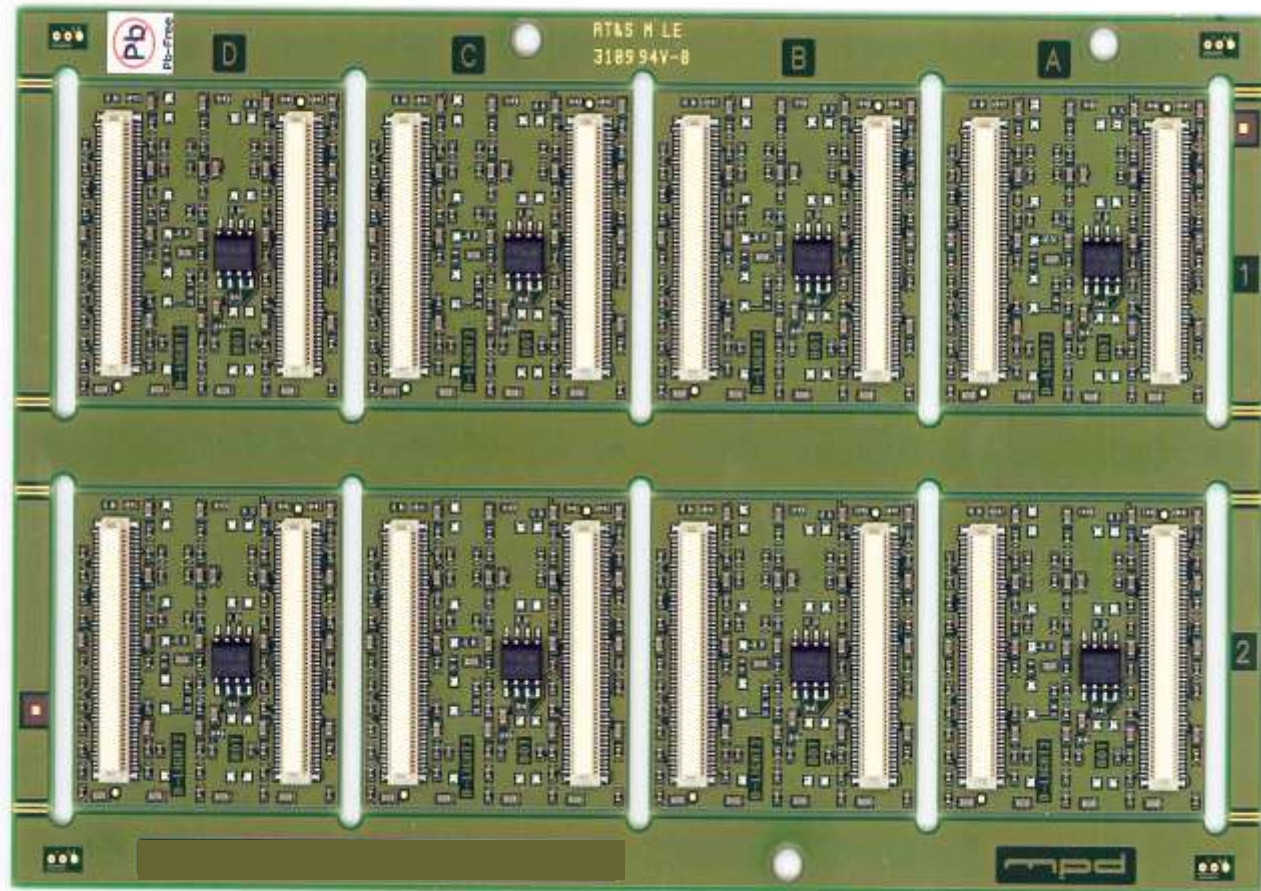
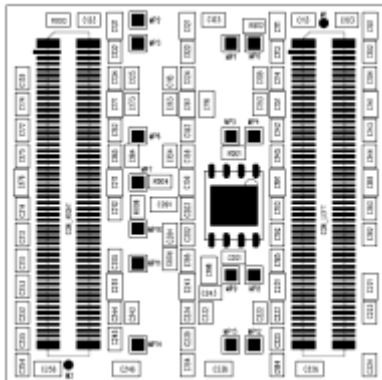


- Boardkrümmung
(IPC 1 % der Boarddicke)

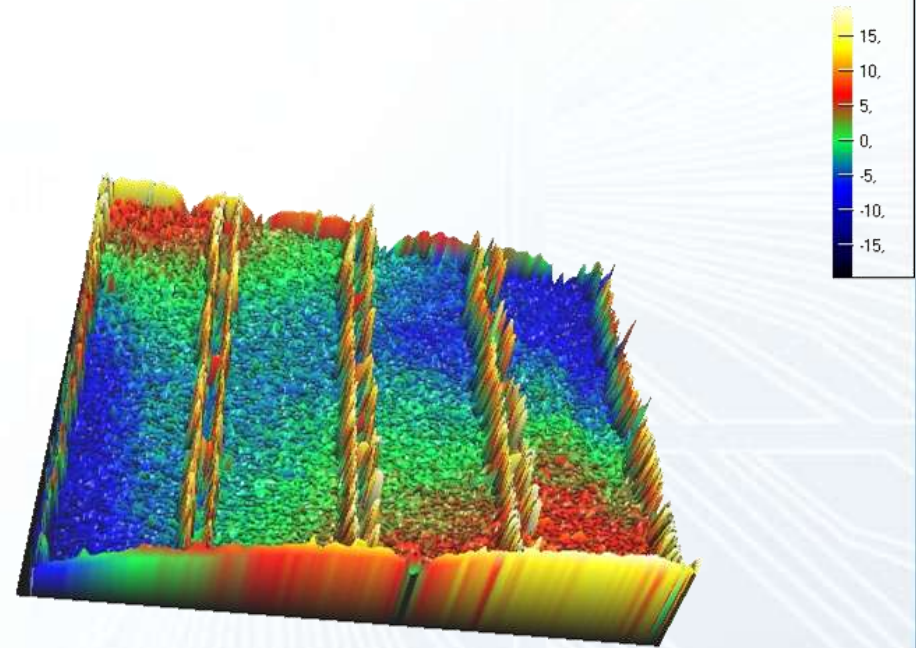
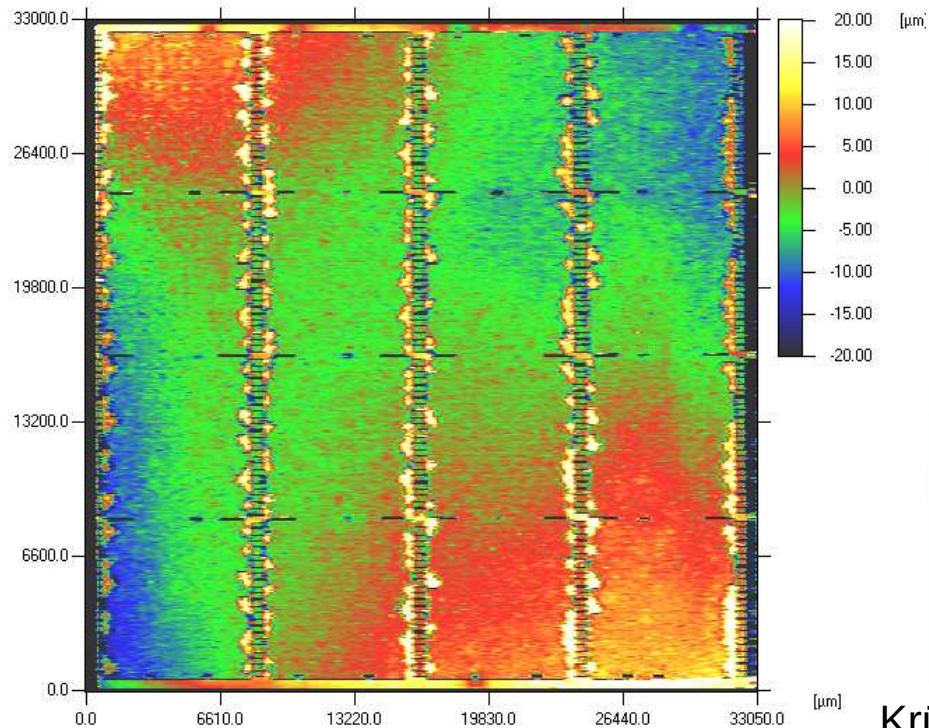


Krümmung max. 15 μm ; leicht konkav

■ SMD-Bestückung



- Boardkrümmung nach SMT



Krümmung max. 27 μm ; leicht konvex

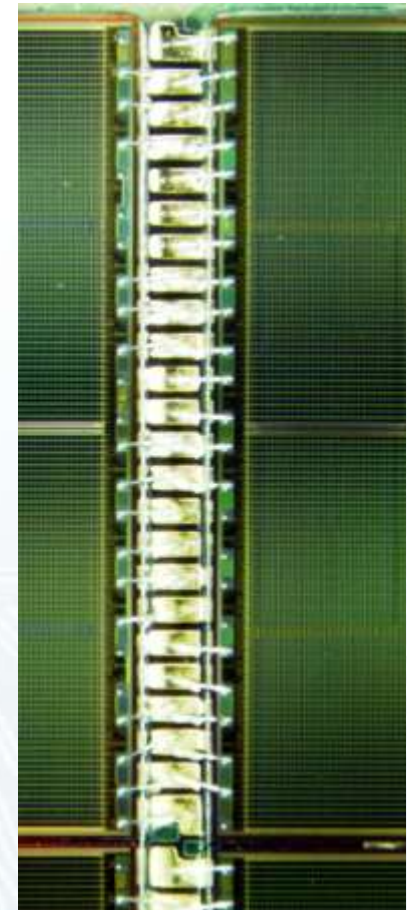
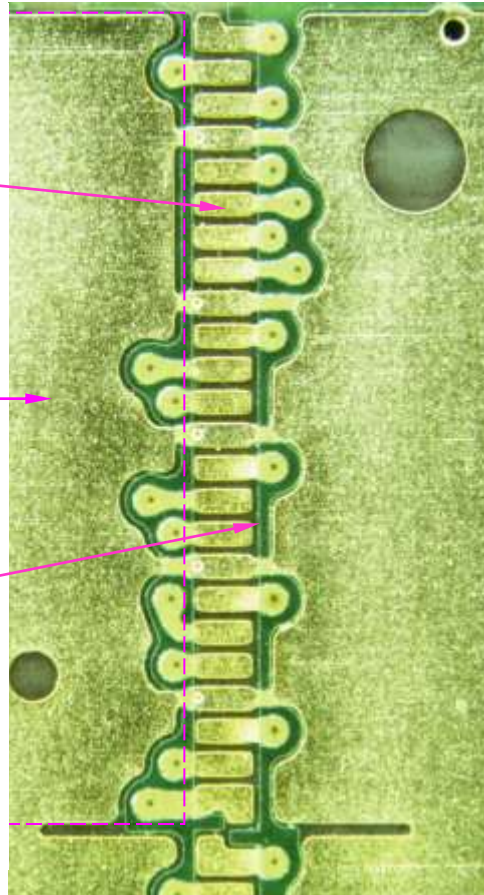
- Chipbonden
 - Stressarme Technologie erforderlich
 - Klebstoff (elektrisch leitfähig)
 - Verfahren
 - Lagegenauigkeit der Dice gemäß Vorgabe ($\pm 25 \mu\text{m}$)
 - Leitende Verbindung zum Board
 - Klebstoffbenetzung lateral begrenzen

- Chipbondpadbereich

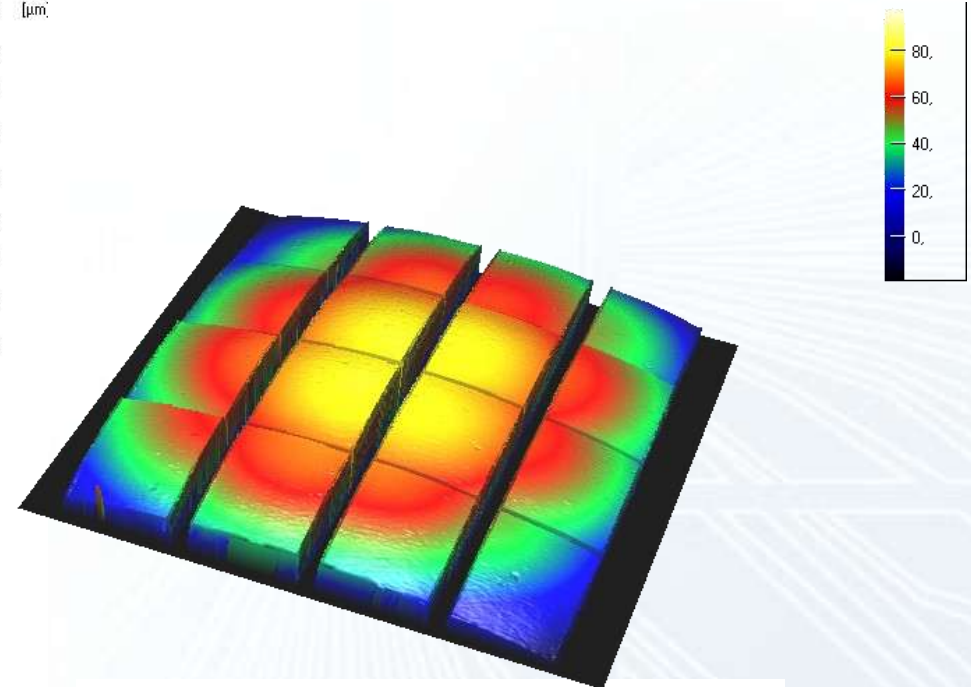
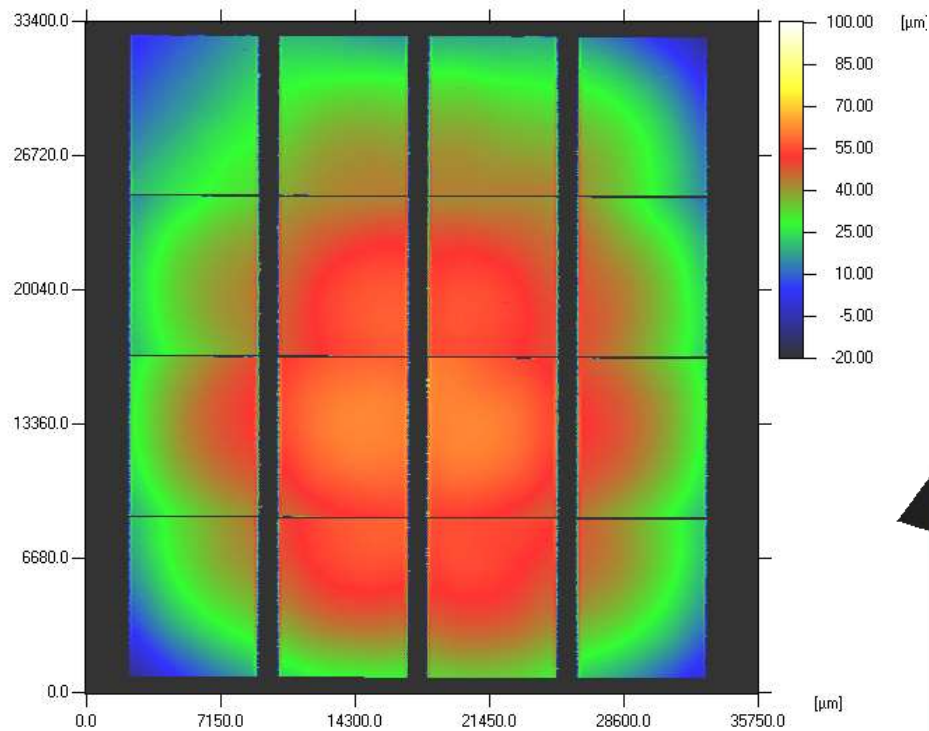
Drahtbondpads

Chipbondpad

Lötstopp -Steg

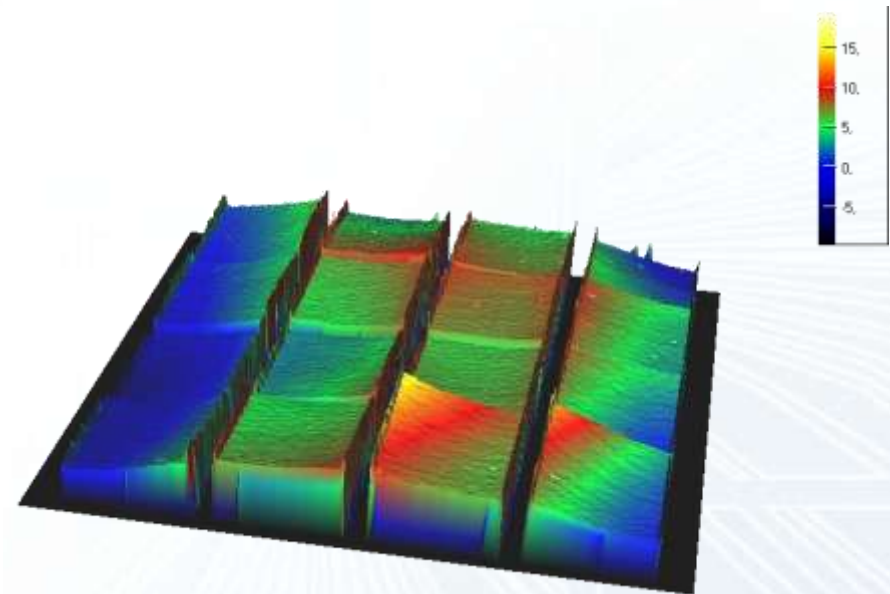
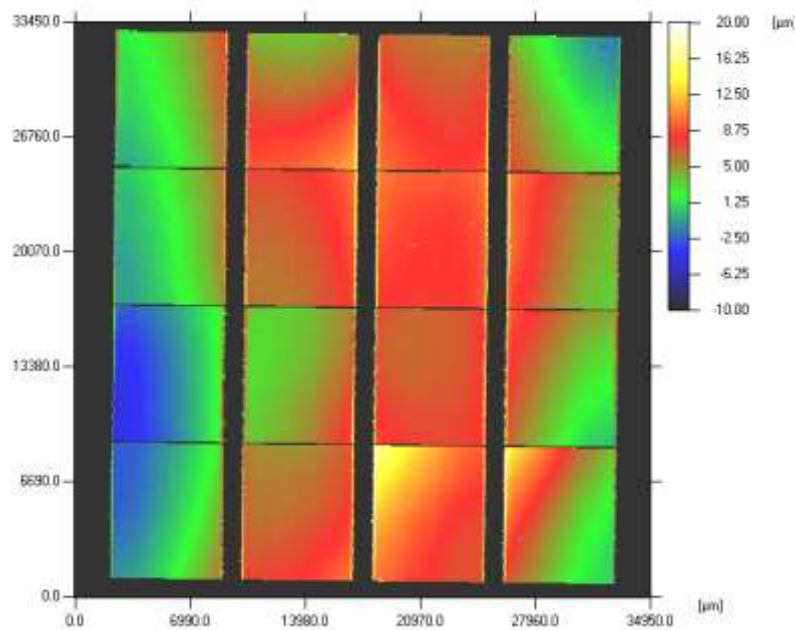


- Modulkrümmung nach Chipbonden



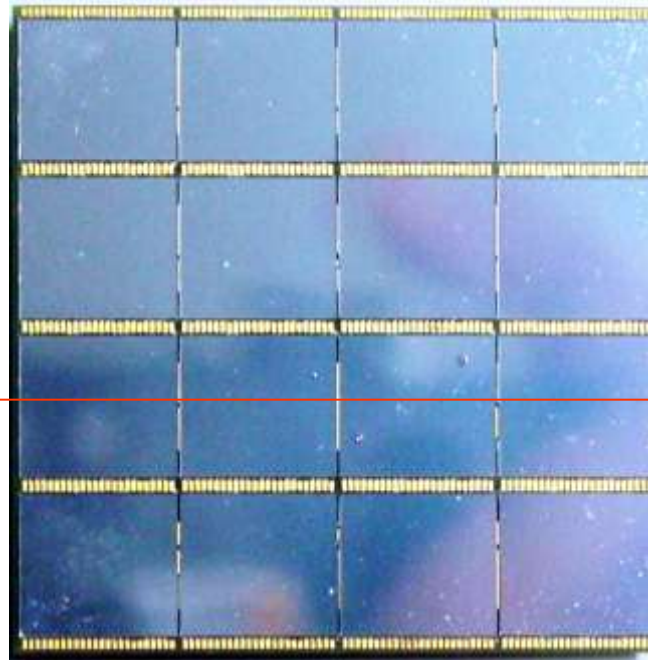
Krümmung max 95 μm ; konvex

- Modulkrümmung nach Chipbonden optimiert (Curing)



Krümmung: max 15 μm ; leicht konvex

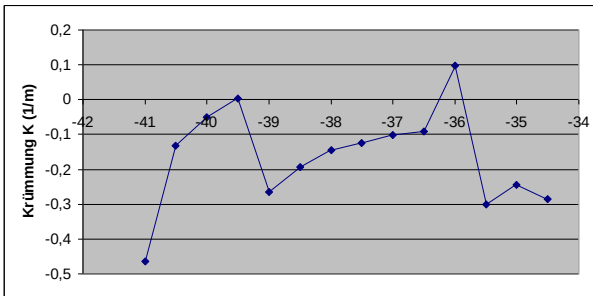
- Chipkrümmung



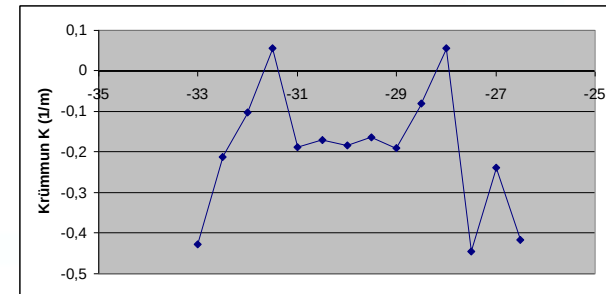
Messlinie für
Chipkrümmung

Laserfokussmessung und röntgenograph. Spannungsmessung

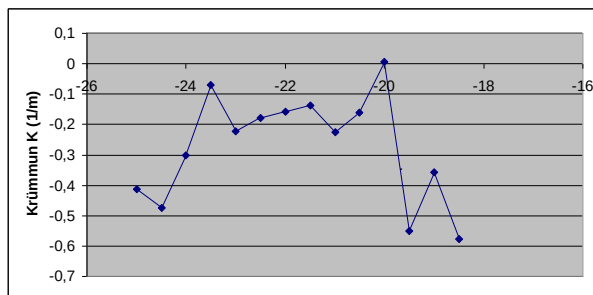
■ Chipkrümmung



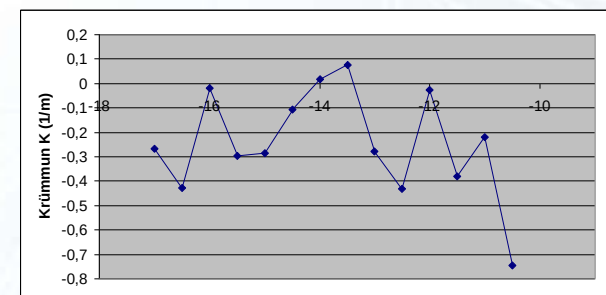
Chip 1



Chip 2

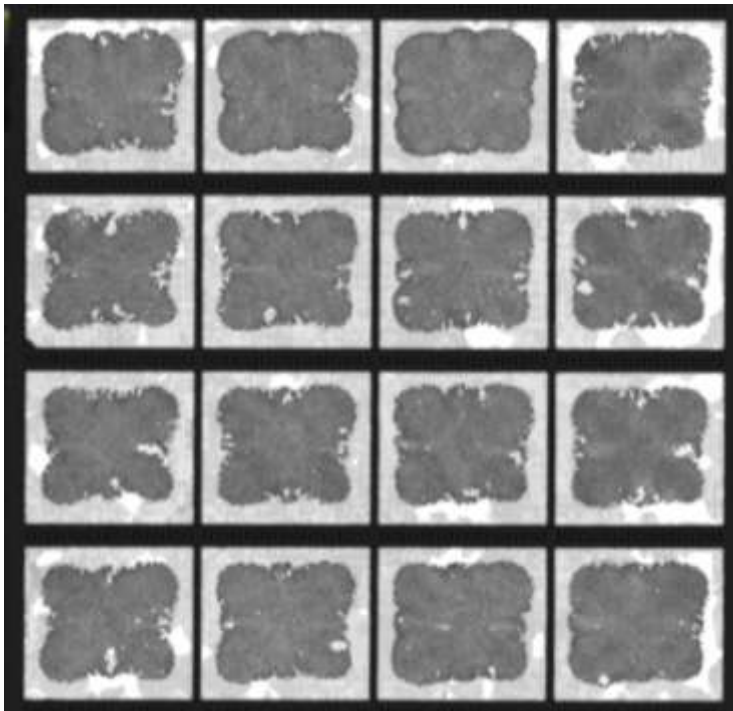


Chip 3

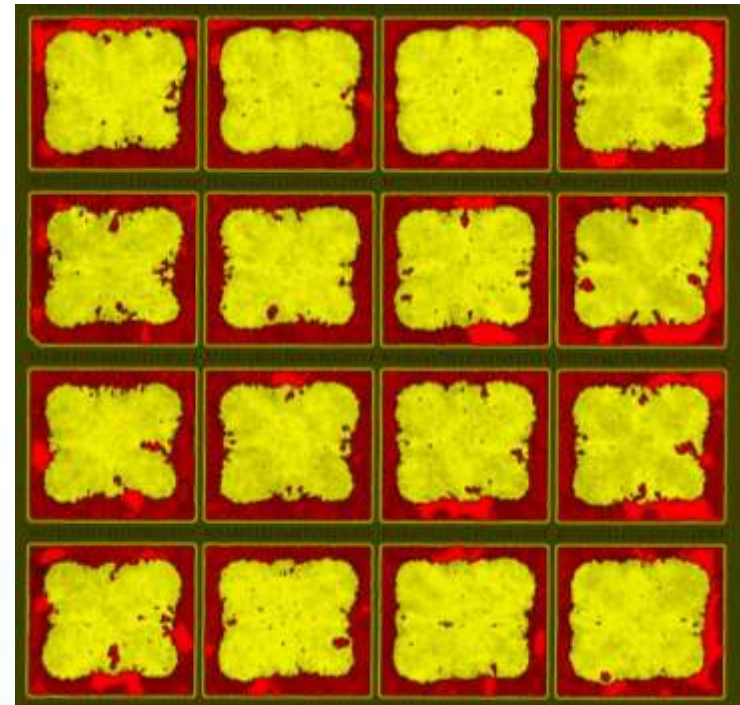


Chip 4

- Klebstoffbild



X - Ray



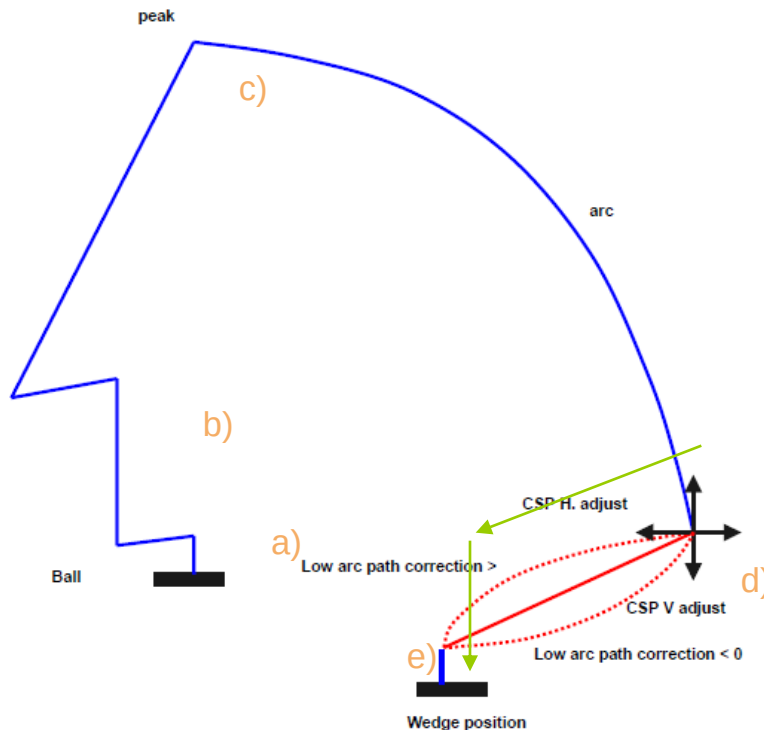
Ultraschallbild

- Drahtbonden
 - US-Bondverfahren
 - AlSi-Draht $\varnothing$ 25 μm
 - Metallisierung Bondpad „Standard“ ENIG (NiAu)
 - Chipdicke **250 μm**
 - TS-Bondverfahren
 - Au-Draht $\varnothing$ 25 μm
 - Metallisierung Bondpad ENIPIG / ENEPIG (NiPdAu)
 - Substrattemperatur > 120 °C
 - Chipdicke **750 μm**
 - Bondgeometrie (Bondloop)
 - Verfahrensoptimierung
 - Bondwerkzeug

■ Bondloop Optimierung

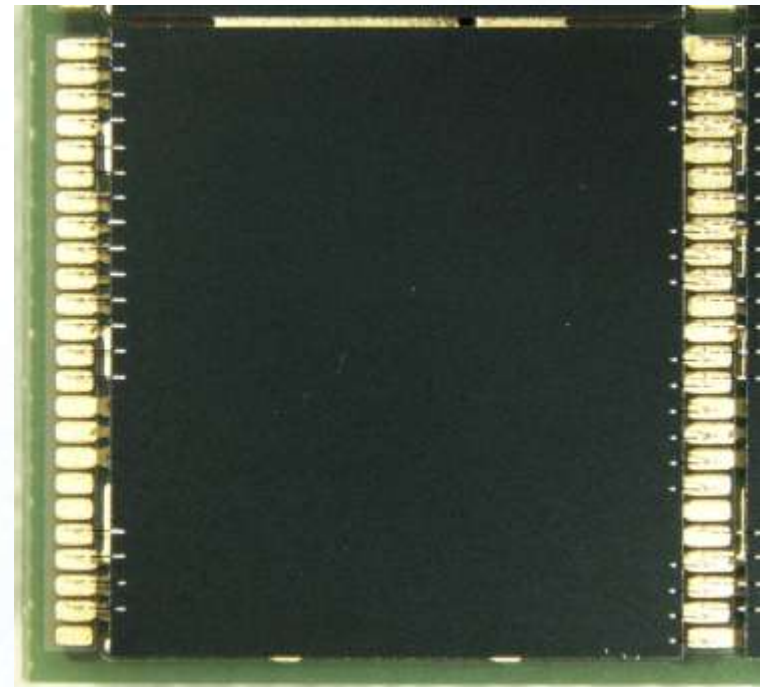
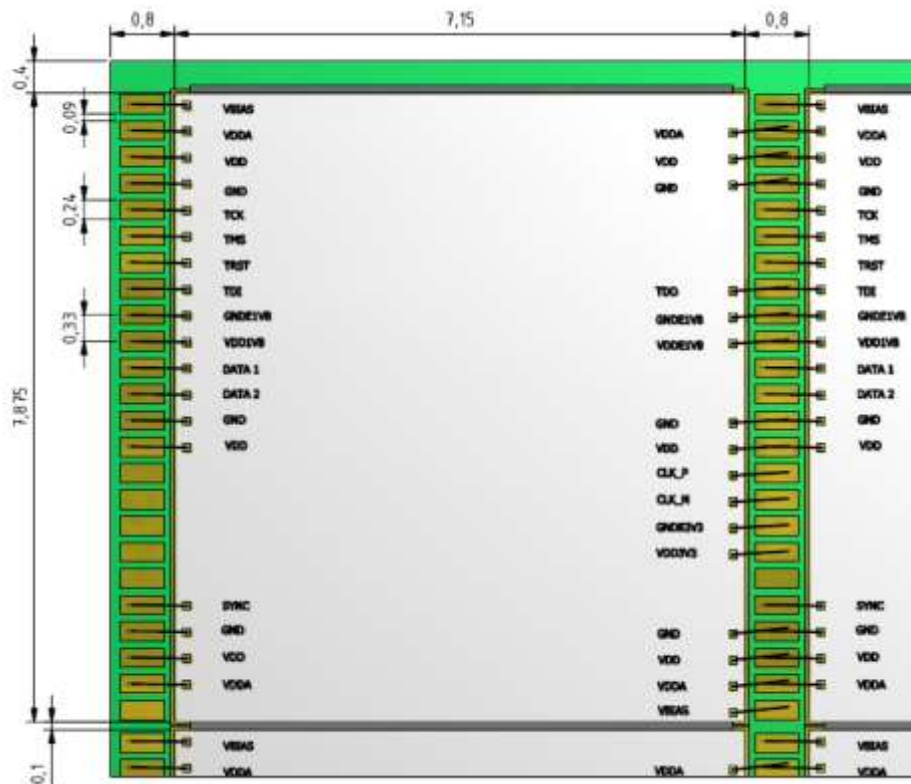
• Theoretischer Ablauf für Bondlooperzeugung

- a) 1. Kontakt erzeugen
- b) Anzahl der „Knicke“ 1) für Bondloop festlegen
- c) Drahtlänge für den Bondloop festlegen
- d) In Richtung 2. Kontakt fahren
- e) 2. Kontakt erzeugen

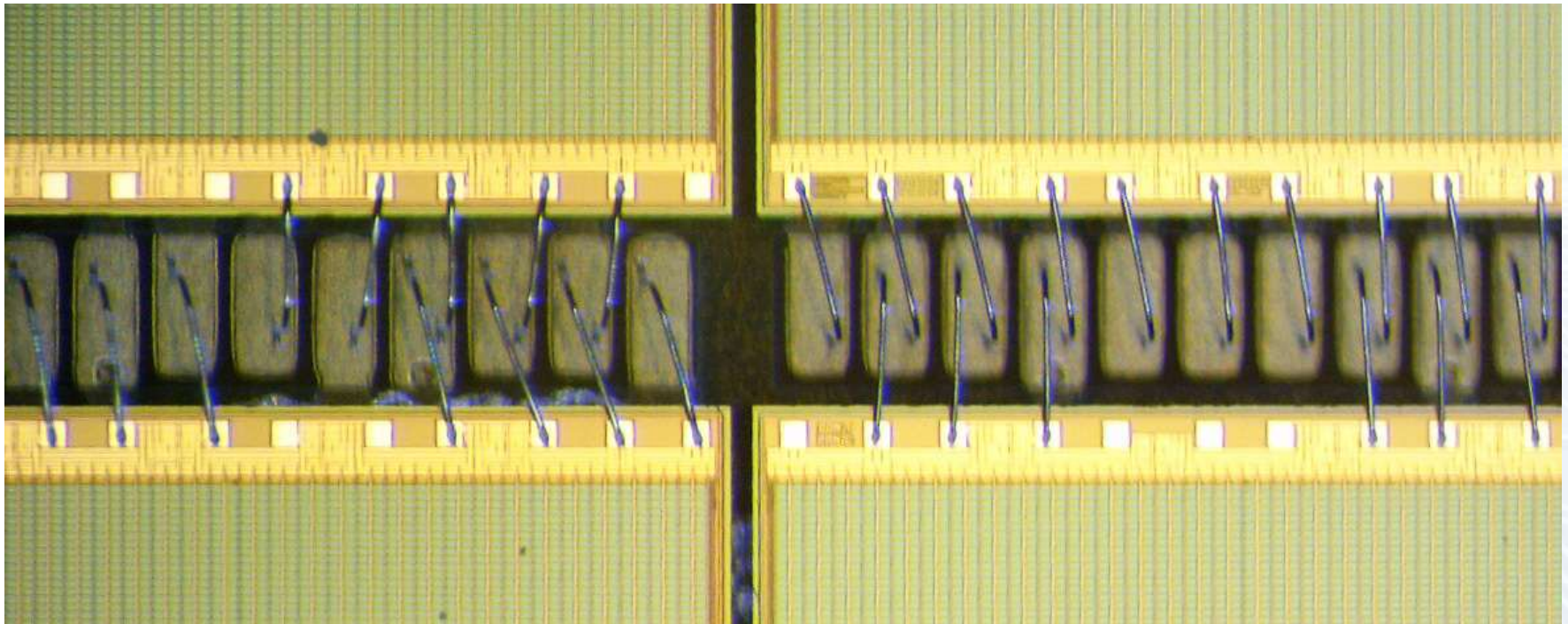


(1) Knick definiert die Biegung im Bondloop

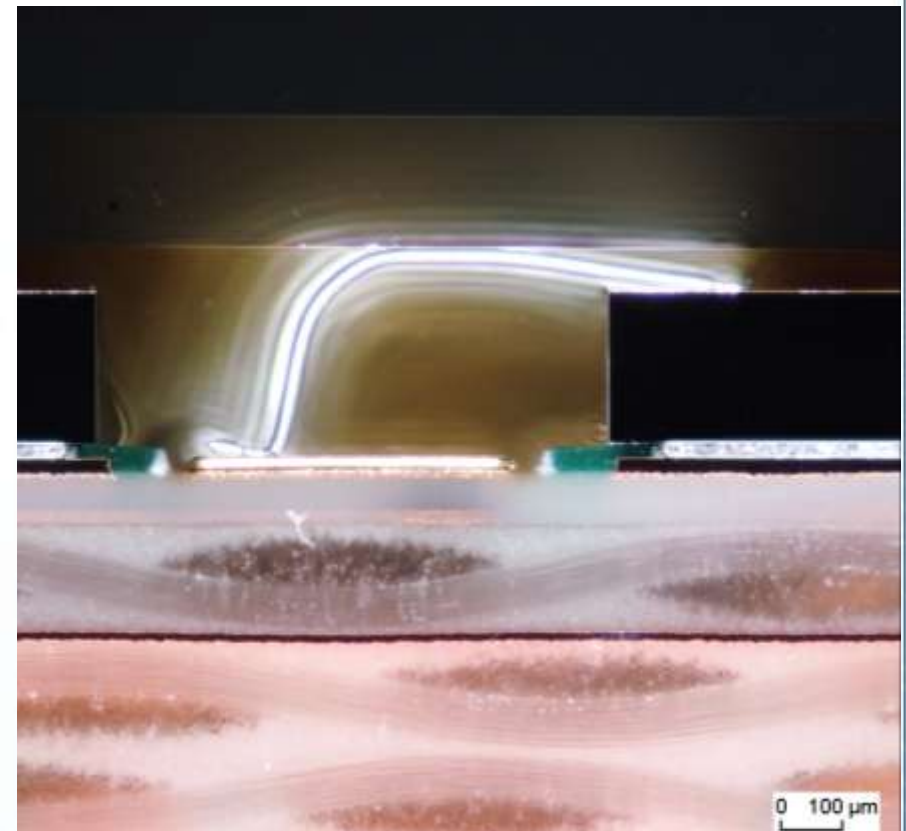
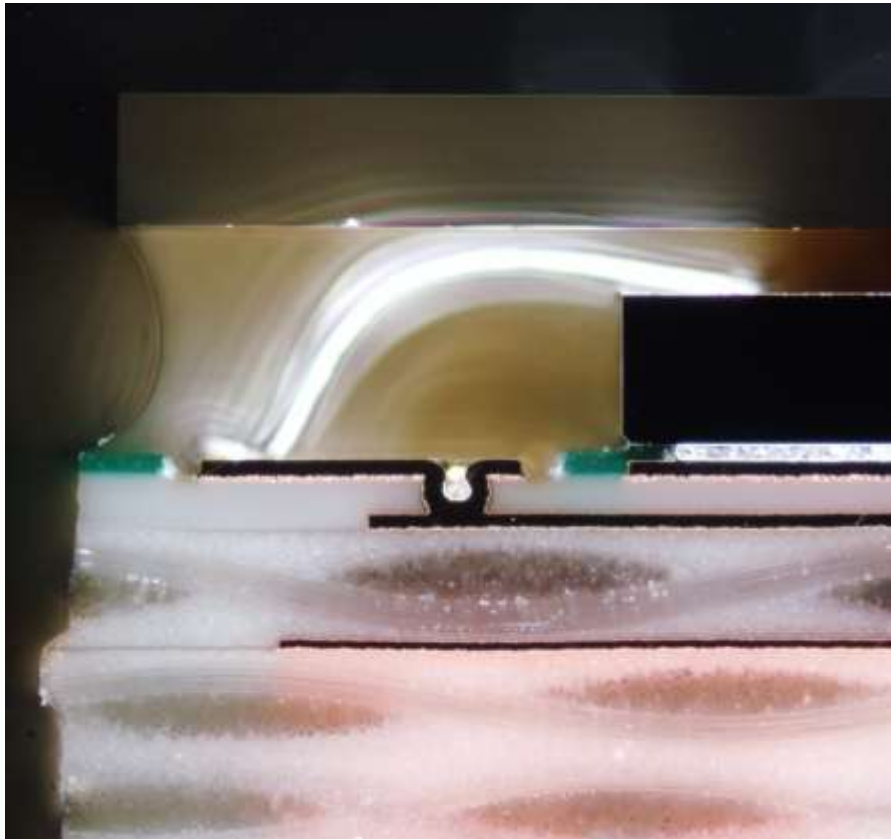
■ Bondlayout



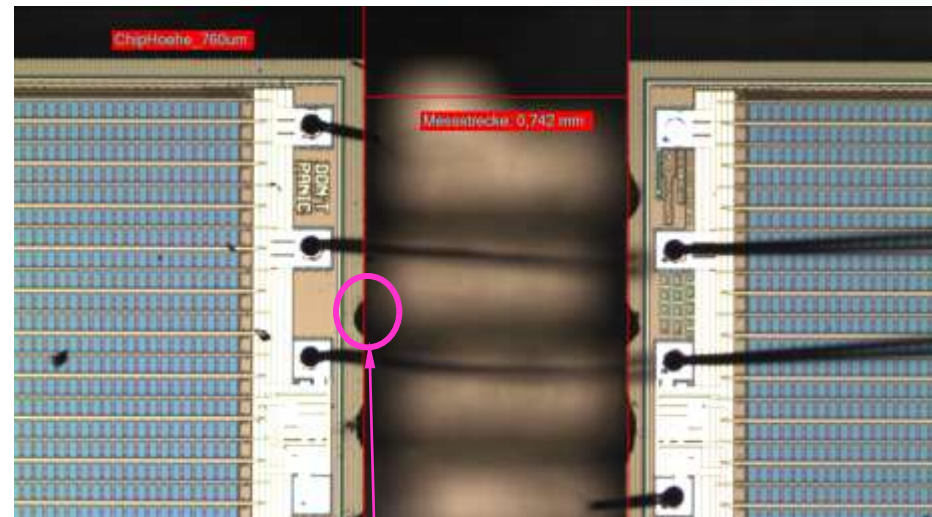
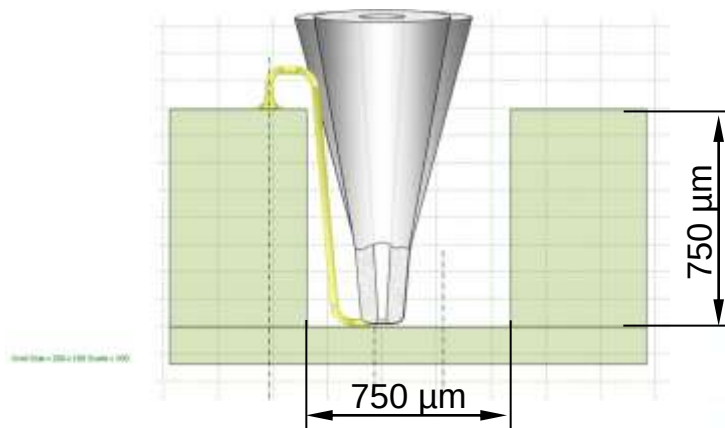
- US - Wedge / Wedge Bonden mit AlSi 1 –Draht / Bondrichtung



- Bondloop AlSi 1-Draht nach Glasmontage

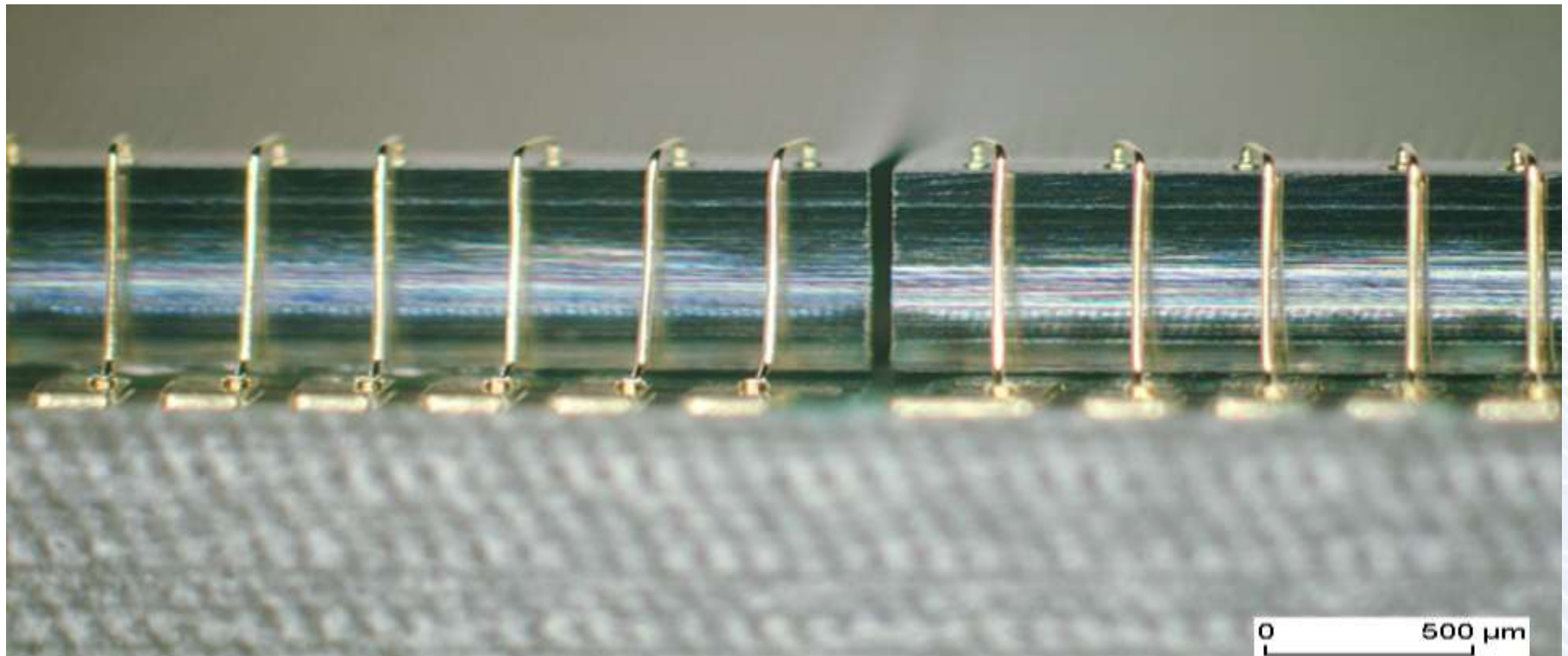


- Thermosonic – Bonden mit Au - Draht
 - Geometrische Verhältnisse / Bondrichtung



Kantenausbruch

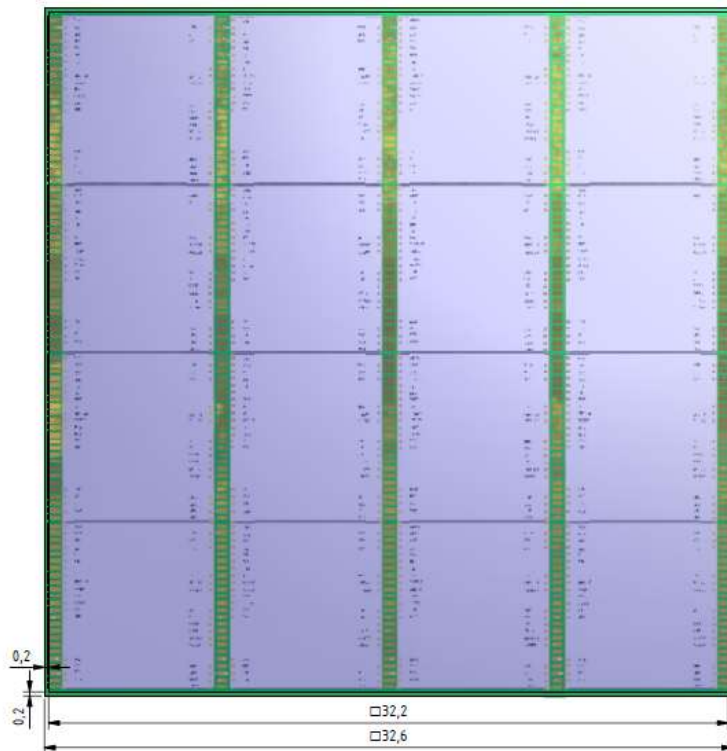
- TS Au-Draht Bondungen



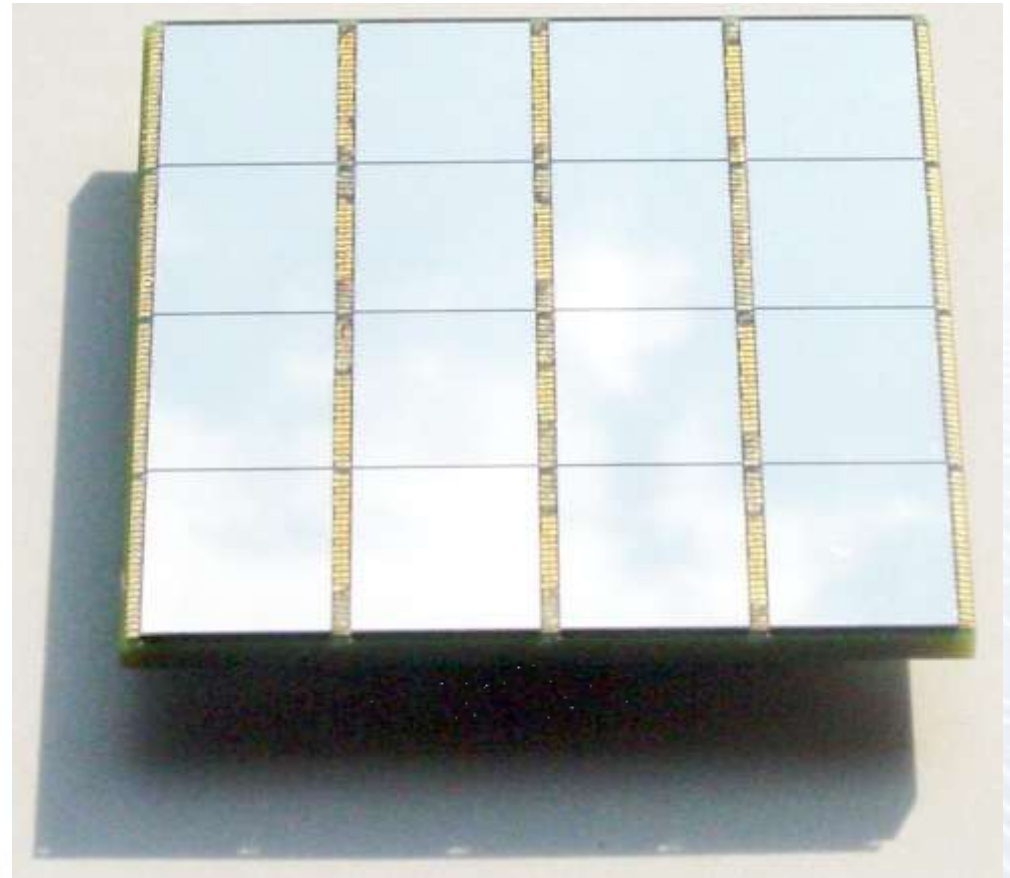


- Glasmontage
 - Glasdicke 0,2 mm $\Rightarrow$ 0,1 mm Handling!
 - Abdeckung der 16 Chips mit einer Glasplatte
 - Geometrie nach Vorgabe
 - Technologie stressarm
 - Klebung blasenarm; optischer Klebstoff

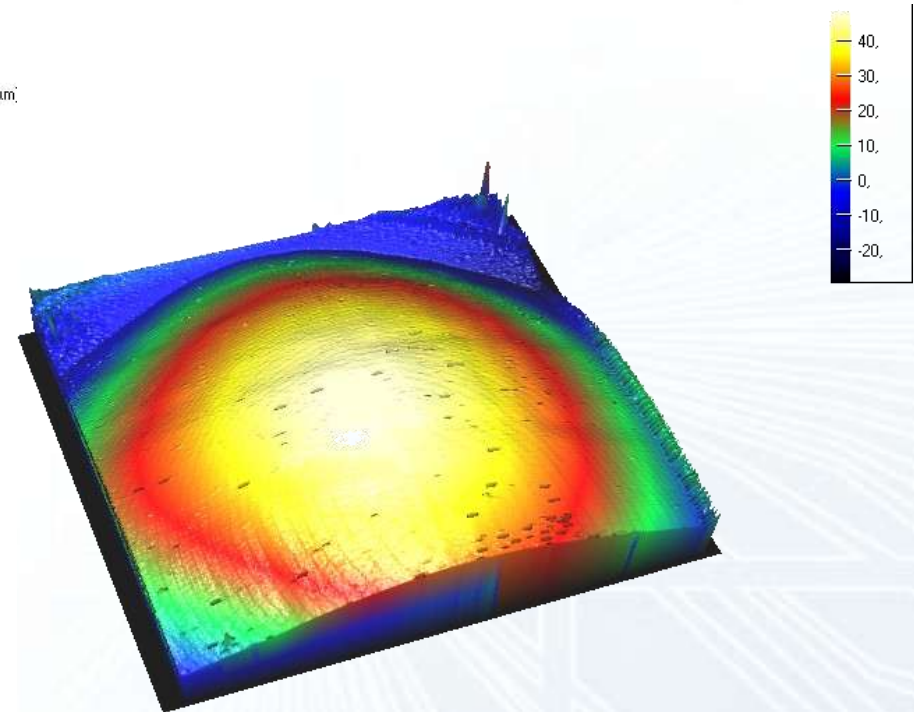
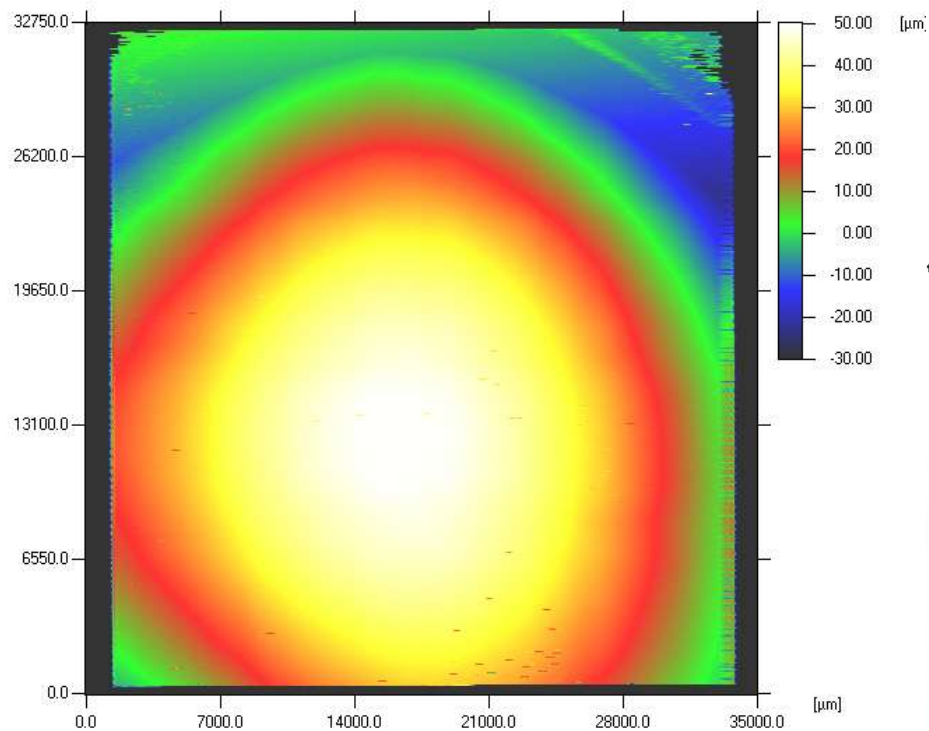
■ Glasmontage



Glasgröße: 32,2 x 32,2 mm²
Glasdicke: 0,1 mm

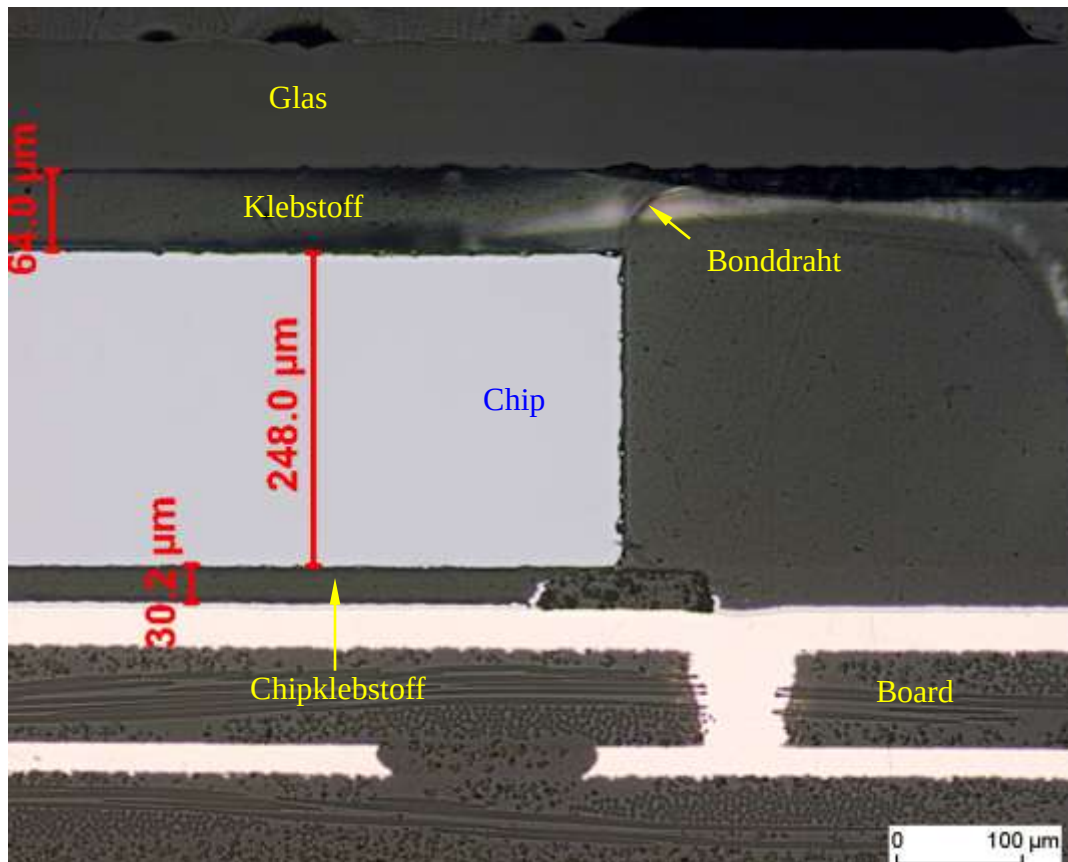


■ Modulkrümmung nach Glasmontage



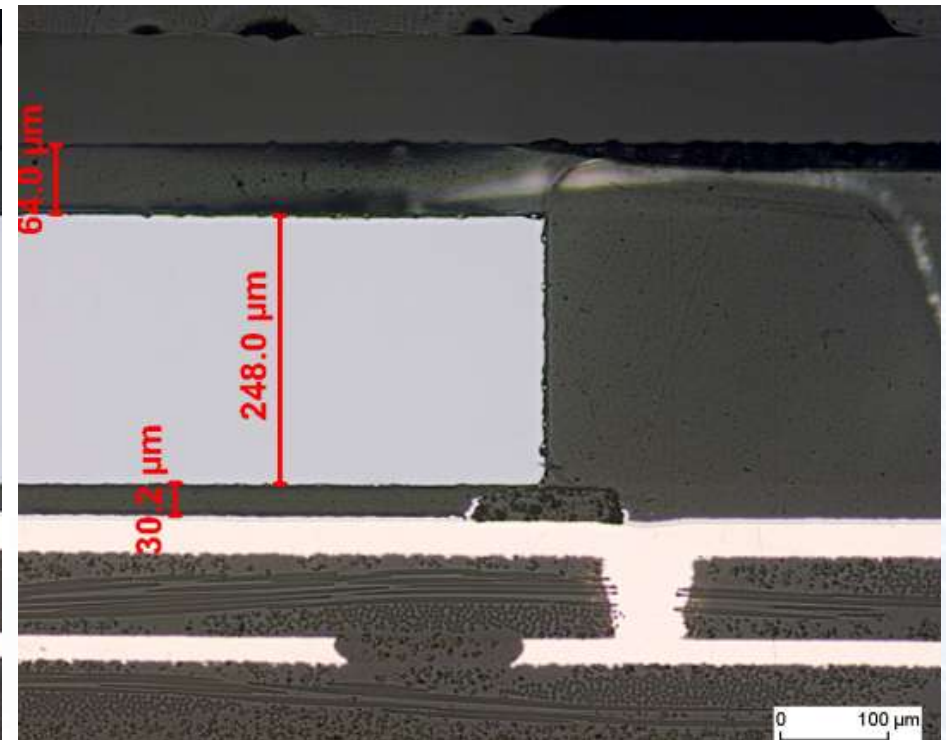
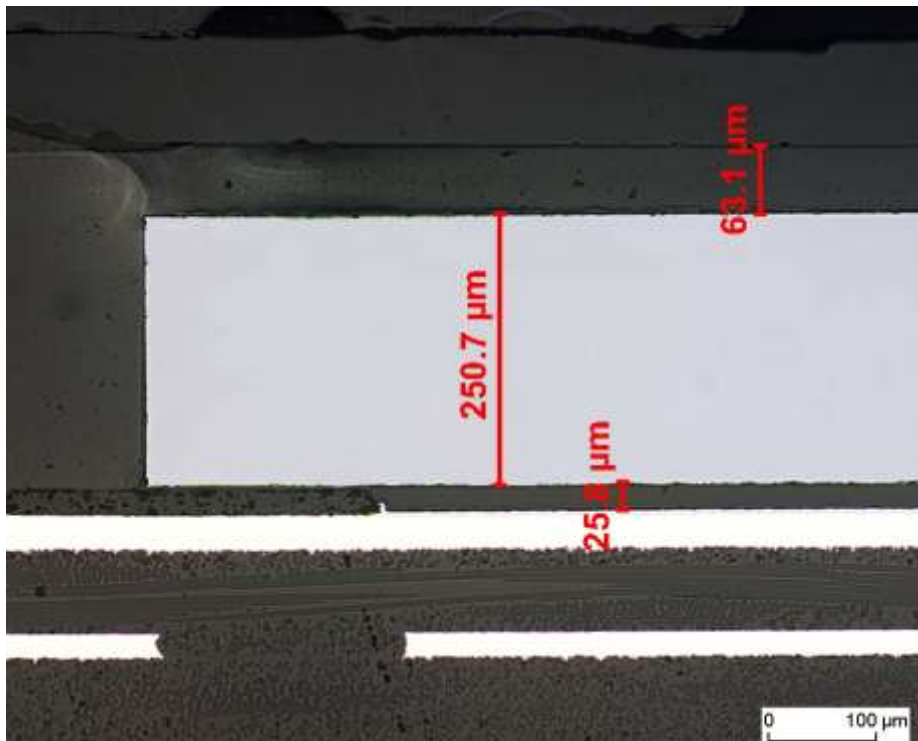
Modulkrümmung max 46 μm , konvex

- Gesamtaufbau im Querschliff

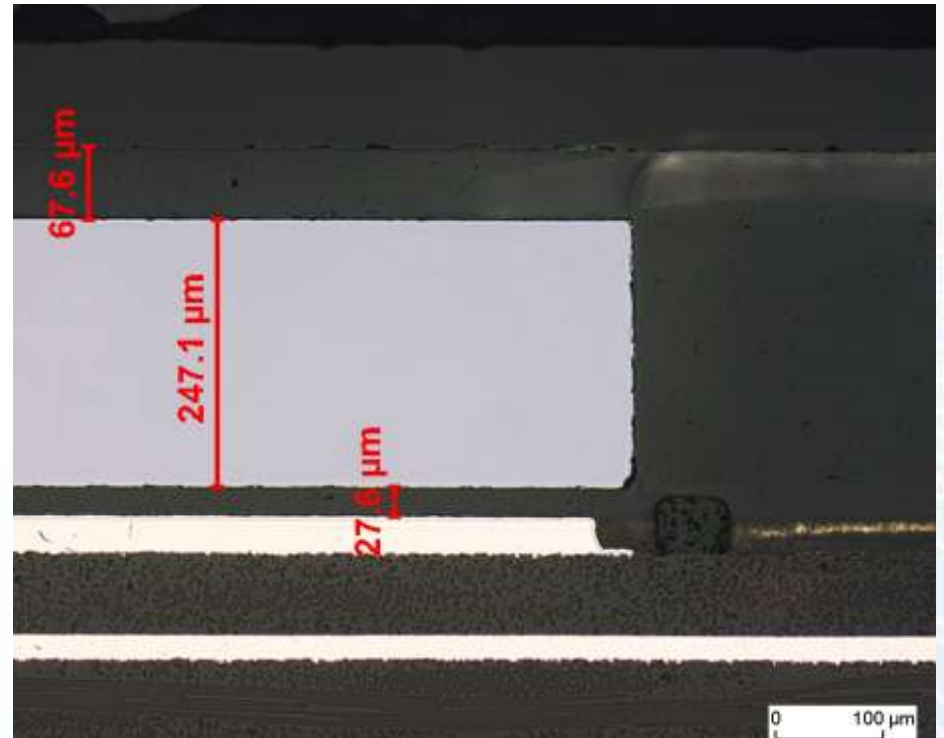


Chip 1 rechts

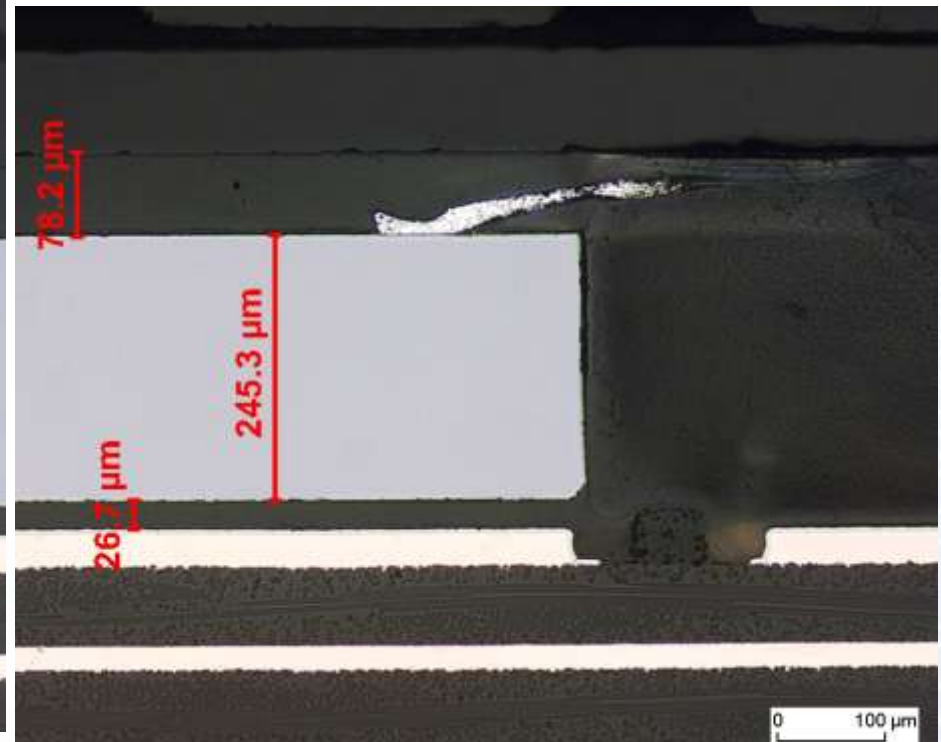
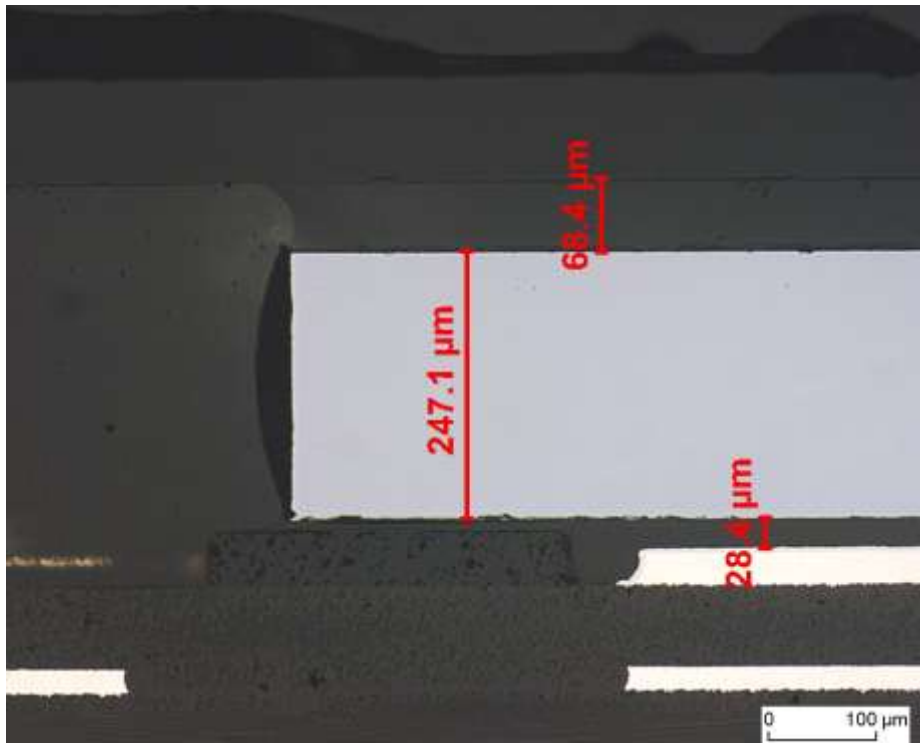
- Chip 1



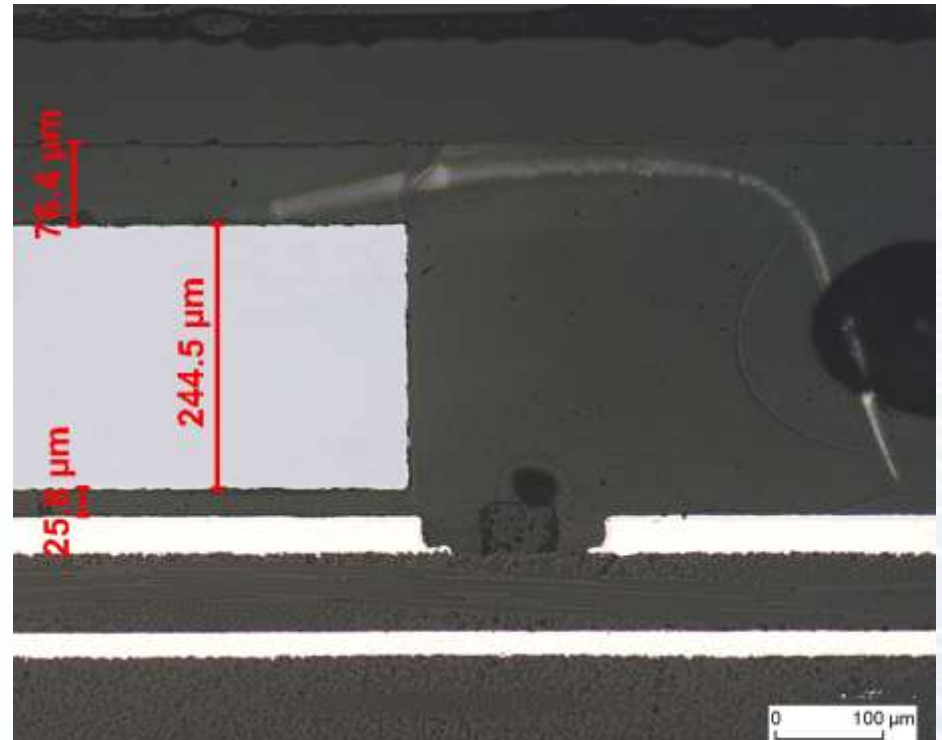
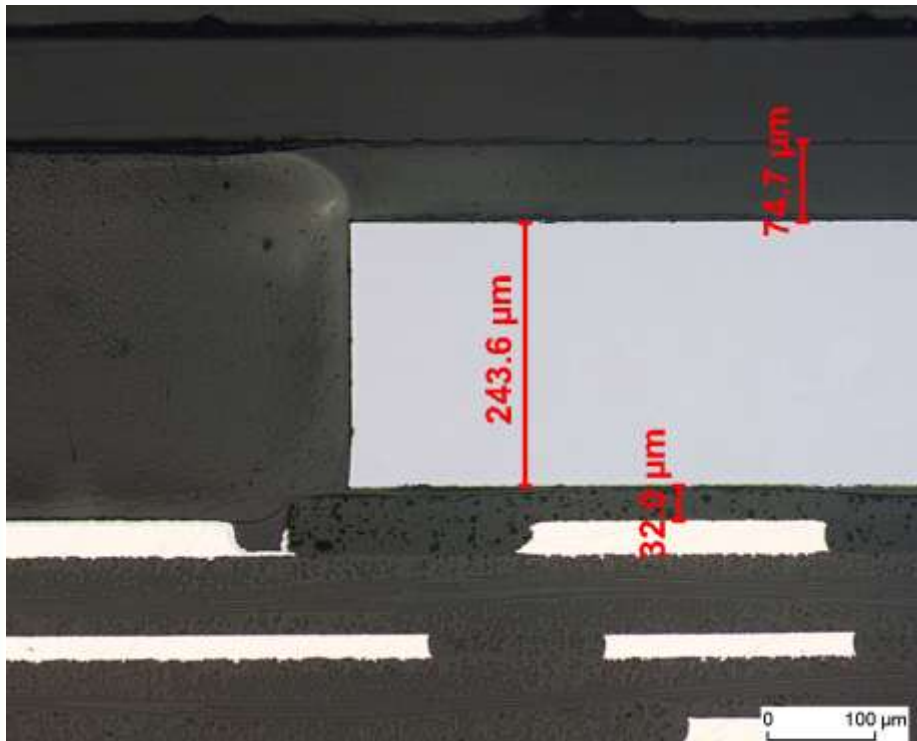
- Chip 2



- Chip 3



- Chip 4



- Zusammenfassung

- Komplexer Aufbau
- Stressarme Technologien notwendig
- Zielstellung konnte erreicht werden
- Entwicklung nur erfolgreich durch gemeinsame Leistung der Produkt- und AVT-Entwickler

